

# Compal Confidential

## NEW50/70/80/90 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M  
ATI Madision/Park

2010-01-07

REV: 1.0

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	Cover Page	
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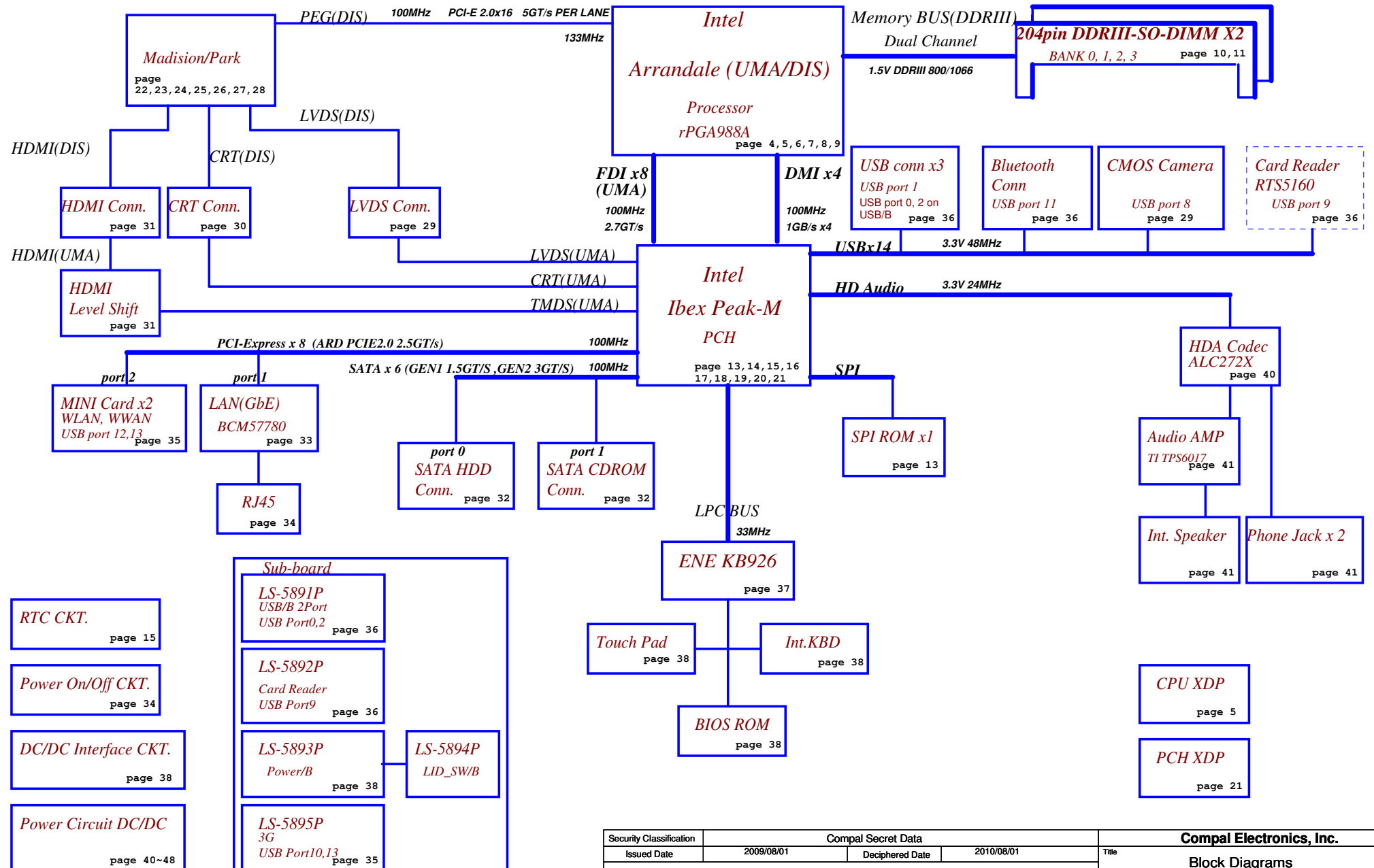
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Model Name : NEW50/70/80/90

File Name : LA5891P

Fan Control  
page 38

Clock Generator  
IDT: 9LVS3199AKLFT  
Realtek: RTM890N-631-VB-GRT  
133/120/100/96/14.318MHZ to PCH  
page 12



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address	
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b	3G & BT Config
DDR DIMM0	1001 000Xb	3G SKU: 3G@
DDR DIMM2	1001 010Xb	BT SKU: BT@
GPU BOM Config		
UMAHD@	VGAHD@	HDMI@
UMA	V	X
VGA	X	V
SG	X	V
NO HDMI	X	X
VRAM BOM Config		
X761@:	X76198BOL01	Park Samsung 512MB
X762@:	X76198BOL02	Park Hynix 512MB
X763@:	X76198BOL03	Madison Samsung 1024MB
X764@:	X76198BOL04	Madison Hynix 1024MB
X765@:	X76198BOL05	Park AMD 512MB
X766@:	X76198BOL06	Madison AMD 1024MB
LED BOM config		
NEW70,80 SKU:	7080@	
NEW50,90 SKU:	5090@	

BOM Config	
UMA W/O HDMI SKU:	BT@/3G@/UMA@/UMAO@
UMA W/ HDMI SKU:	BT@/3G@/UMA@/UMAO@/HDMI@/UMAHD@
Discrete W/O HDMI SKU:	BT@/3G@/DIS@/DISO@/VGA@
Discrete W/ HDMI SKU:	BT@/3G@/DIS@/DISO@/VGA@/HDMI@/VGAHD@
Switchable W/O HDMI SKU:	BT@/3G@/DIS@/UMA@/VGA@/SG@
Switchable W HDMI SKU:	BT@/3G@/DIS@/UMA@/VGA@/SG@/HDMI@/VGAHD@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMAO@
Discrete	DIS@
Discrete Only	DISO@
GPU ALL Components	VGA@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
UMA HDMI	UMAHD@
Discrete HDMI	VGAHD@
UMA & DIS POP HDMI	HDMI@
GPU Madision	MADI@
GPU Park	PARK@
NEW70,80 LED	7080@
NEW50,90 LED	5090@

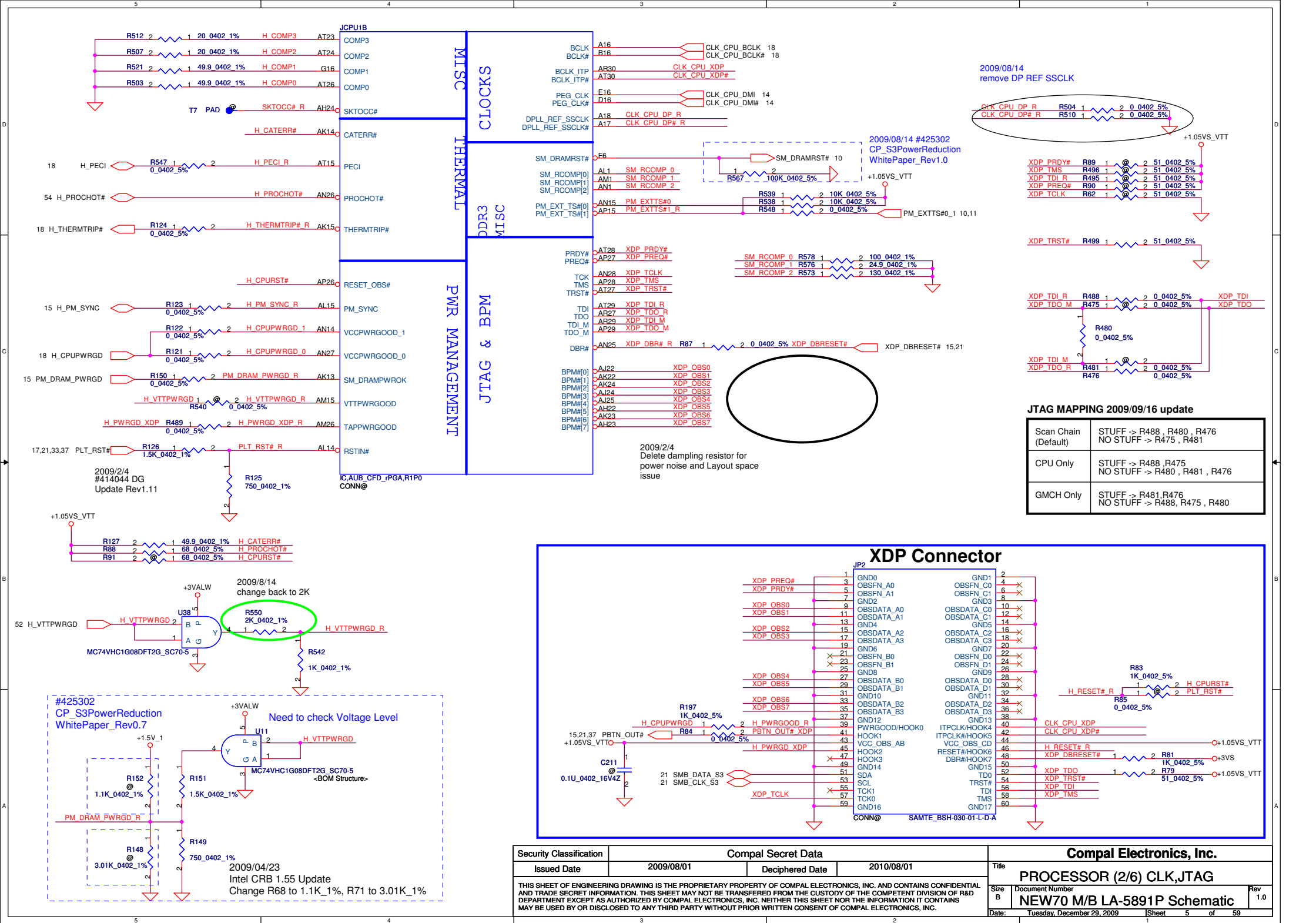
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
7			
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

X76@			ID2: VRAM Size		
ID3 , ID1 : VRAM Vender			Location		
VRAM			VRAM_ID1		
Samsung			VRAM_ID2		
HYNIX			8PCS 64Mx16		
AMD			4PCS 64Mx16		
VRAM P/N :			R482		
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)			R483		
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V )					
AMD : SA00003PF20 (S IC D3 23EY2387MB-12)					

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10 DDR\_A\_D[0..63]  
10 DDR\_A\_DM[0..7]  
10 DDR\_A\_DQS[0..7]  
10 DDR\_A\_MA[0..15]

JCPU1C

DDR A D0 A10  
DDR A D1 C10  
DDR A D2 C7  
DDR A D3 A7  
DDR A D4 B10  
DDR A D5 D10  
DDR A D6 E10  
DDR A D7 A8  
DDR A D8 D8  
DDR A D9 F10  
DDR A D10 E6  
DDR A D11 E7  
DDR A D12 E9  
DDR A D13 B7  
DDR A D14 E7  
DDR A D15 C6  
DDR A D16 H10  
DDR A D17 G8  
DDR A D18 K7  
DDR A D19 J8  
DDR A D20 G7  
DDR A D21 G10  
DDR A D22 J7  
DDR A D23 J10  
DDR A D24 L7  
DDR A D25 M6  
DDR A D26 M8  
DDR A D27 L9  
DDR A D28 L6  
DDR A D29 K8  
DDR A D30 N8  
DDR A D31 P9  
DDR A D32 AH5  
DDR A D33 AF5  
DDR A D34 AK6  
DDR A D35 AK7  
DDR A D36 AF6  
DDR A D37 AG5  
DDR A D38 AJ7  
DDR A D39 AJ6  
DDR A D40 AJ10  
DDR A D41 AJ9  
DDR A D42 AL10  
DDR A D43 AK12  
DDR A D44 AK8  
DDR A D45 AL7  
DDR A D46 AK11  
DDR A D47 AL8  
DDR A D48 AN8  
DDR A D49 AM10  
DDR A D50 AR11  
DDR A D51 AL11  
DDR A D52 AM9  
DDR A D53 AN9  
DDR A D54 AT11  
DDR A D55 AP12  
DDR A D56 AM12  
DDR A D57 AN12  
DDR A D58 AM13  
DDR A D59 AT14  
DDR A D60 AT12  
DDR A D61 AL13  
DDR A D62 AR14  
DDR A D63 AP14

10 DDR\_A\_BS0  
10 DDR\_A\_BS1  
10 DDR\_A\_BS2

10 DDR\_A\_CAS#  
10 DDR\_A\_RAS#  
10 DDR\_A\_WE#

DDR SYSTEM MEMORY A

SA\_CK[0] AA6  
SA\_CK#0 AA7  
SA\_CKE[0] P7  
SA\_CK[1] Y6  
SA\_CK#1 Y5  
SA\_CKE[1] P6  
SA\_CS#0 AE2  
SA\_CS#1 AE8  
SA\_ODT[0] AD8  
SA\_ODT[1] AF9  
SA\_DM[0] B9  
SA\_DM[1] D7  
SA\_DM[2] L7  
SA\_DM[3] M7  
SA\_DM[4] AG6  
SA\_DM[5] AM7  
SA\_DM[6] AN10  
SA\_DM[7] AN13  
SA\_DQS#0 C9  
SA\_DQS#1 C8  
SA\_DQS#2 C9  
SA\_DQS#3 AH7  
SA\_DQS#4 AK9  
SA\_DQS#5 AP11  
SA\_DQS#6 AT13  
SA\_DQS#7  
SA\_DQS[0] C8  
SA\_DQS[1] F9  
SA\_DQS[2] L9  
SA\_DQS[3] M9  
SA\_DQS[4] AH8  
SA\_DQS[5] AK10  
SA\_DQS[6] AN11  
SA\_DQS[7] AR13  
SA\_MA[0] Y3  
SA\_MA[1] W1  
SA\_MA[2] AA8  
SA\_MA[3] AA3  
SA\_MA[4] V1  
SA\_MA[5] AA9  
SA\_MA[6] V8  
SA\_MA[7] T1  
SA\_MA[8] Y9  
SA\_MA[9] U6  
SA\_MA[10] AD4  
SA\_MA[11] U3  
SA\_MA[12] AG8  
SA\_MA[13] T3  
SA\_MA[14] V9  
SA\_MA[15]

IC:AUB\_CFD\_rPGA,R1P0  
CONN@

11 DDR\_B\_D[0..63]  
11 DDR\_B\_DM[0..7]  
11 DDR\_B\_DQS[0..7]  
11 DDR\_B\_MA[0..15]

JCPU1D

DDR B D0 B5  
DDR B D1 A5  
DDR B D2 C3  
DDR B D3 B3  
DDR B D4 E4  
DDR B D5 A6  
DDR B D6 C4  
DDR B D7 C4  
DDR B D8 D1  
DDR B D9 D2  
DDR B D10 F2  
DDR B D11 F1  
DDR B D12 C2  
DDR B D13 F5  
DDR B D14 F3  
DDR B D15 G4  
DDR B D16 H6  
DDR B D17 G2  
DDR B D18 J6  
DDR B D19 J3  
DDR B D20 G1  
DDR B D21 G5  
DDR B D22 J2  
DDR B D23 J1  
DDR B D24 J5  
DDR B D25 K2  
DDR B D26 M1  
DDR B D27 M5  
DDR B D28 K5  
DDR B D29 K4  
DDR B D30 M4  
DDR B D31 N5  
DDR B D32 AG1  
DDR B D33 AG1  
DDR B D34 AJ3  
DDR B D35 AK1  
DDR B D36 AG4  
DDR B D37 AG3  
DDR B D38 AJ4  
DDR B D39 AH4  
DDR B D40 AK3  
DDR B D41 AK4  
DDR B D42 AM6  
DDR B D43 AN2  
DDR B D44 AK5  
DDR B D45 AK2  
DDR B D46 AM4  
DDR B D47 AM3  
DDR B D48 AP3  
DDR B D49 AN5  
DDR B D50 AT4  
DDR B D51 AN6  
DDR B D52 AN4  
DDR B D53 AN5  
DDR B D54 AT5  
DDR B D55 AT6  
DDR B D56 AN7  
DDR B D57 AP6  
DDR B D58 AP8  
DDR B D59 AT9  
DDR B D60 AT7  
DDR B D61 AP9  
DDR B D62 AR10  
DDR B D63 AT10

11 DDR\_B\_BS0  
11 DDR\_B\_BS1  
11 DDR\_B\_BS2

11 DDR\_B\_CAS#  
11 DDR\_B\_RAS#  
11 DDR\_B\_WE#

DDR SYSTEM MEMORY - B

SB\_CK[0] W8  
SB\_CK#0 W9  
SB\_CKE[0] M3  
SB\_CK[1] V7  
SB\_CK#1 V6  
SB\_CKE[1] M2  
SB\_CS#0 AB8  
SB\_CS#1 AD6  
SB\_ODT[0] AC7  
SB\_ODT[1] AD1  
SB\_DM[0] D4  
SB\_DM[1] E1  
SB\_DM[2] H3  
SB\_DM[3] K1  
SB\_DM[4] AH1  
SB\_DM[5] AL2  
SB\_DM[6] AR4  
SB\_DM[7] AT8  
SB\_DQS#0 D5  
SB\_DQS#1 E4  
SB\_DQS#2 D4  
SB\_DQS#3 L4  
SB\_DQS#4 AH2  
SB\_DQS#5 AL4  
SB\_DQS#6 AR5  
SB\_DQS#7 AR8  
SB\_DQS[0] C5  
SB\_DQS[1] E3  
SB\_DQS[2] H4  
SB\_DQS[3] M5  
SB\_DQS[4] AG2  
SB\_DQS[5] AL5  
SB\_DQS[6] AP5  
SB\_DQS[7] AR7  
SB\_MA[0] U5  
SB\_MA[1] V2  
SB\_MA[2] T5  
SB\_MA[3] V3  
SB\_MA[4] B1  
SB\_MA[5] T8  
SB\_MA[6] R2  
SB\_MA[7] B6  
SB\_MA[8] B4  
SB\_MA[9] R5  
SB\_MA[10] AR5  
SB\_MA[11] P3  
SB\_MA[12] R3  
SB\_MA[13] AF7  
SB\_MA[14] P5  
SB\_MA[15] N1

DDR\_B\_CLK0 11  
DDR\_B\_CLK0# 11  
DDR\_B\_CKE0 11  
DDR\_B\_CLK1 11  
DDR\_B\_CLK1# 11  
DDR\_B\_CKE1 11

DDR\_B\_CS0# 11  
DDR\_B\_CS1# 11

DDR\_B\_ODT0 11  
DDR\_B\_ODT1 11

DDR B DM0  
DDR B DM1  
DDR B DM2  
DDR B DM3  
DDR B DM4  
DDR B DM5  
DDR B DM6  
DDR B DM7

DDR B DQS#0  
DDR B DQS#1  
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DDR B DQS#7

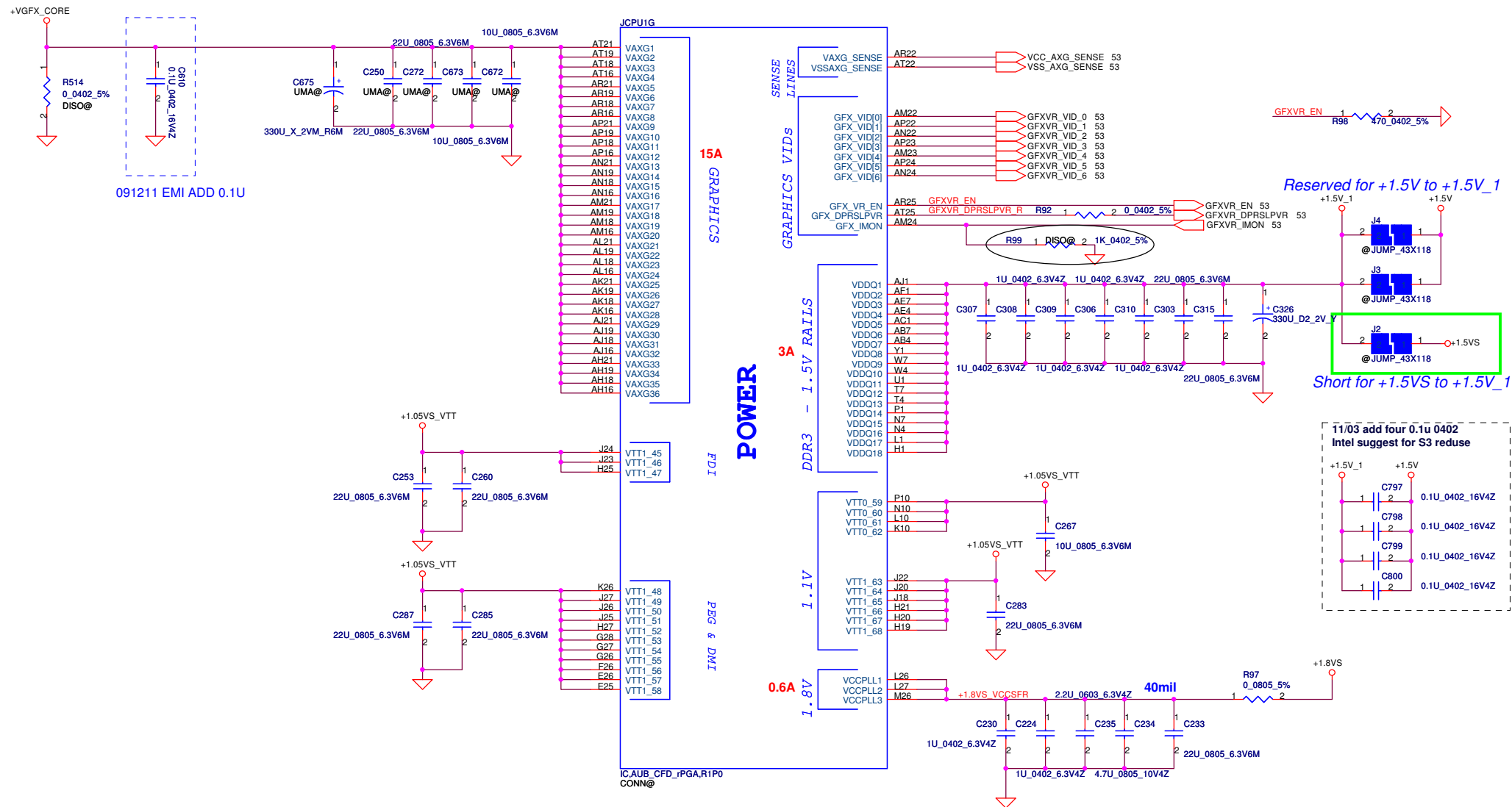
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DDR B DQS5  
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DDR B DQS7

DDR B MA0  
DDR B MA1  
DDR B MA2  
DDR B MA3  
DDR B MA4  
DDR B MA5  
DDR B MA6  
DDR B MA7  
DDR B MA8  
DDR B MA9  
DDR B MA10  
DDR B MA11  
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DDR B MA13  
DDR B MA14  
DDR B MA15

IC:AUB\_CFD\_rPGA,R1P0  
CONN@

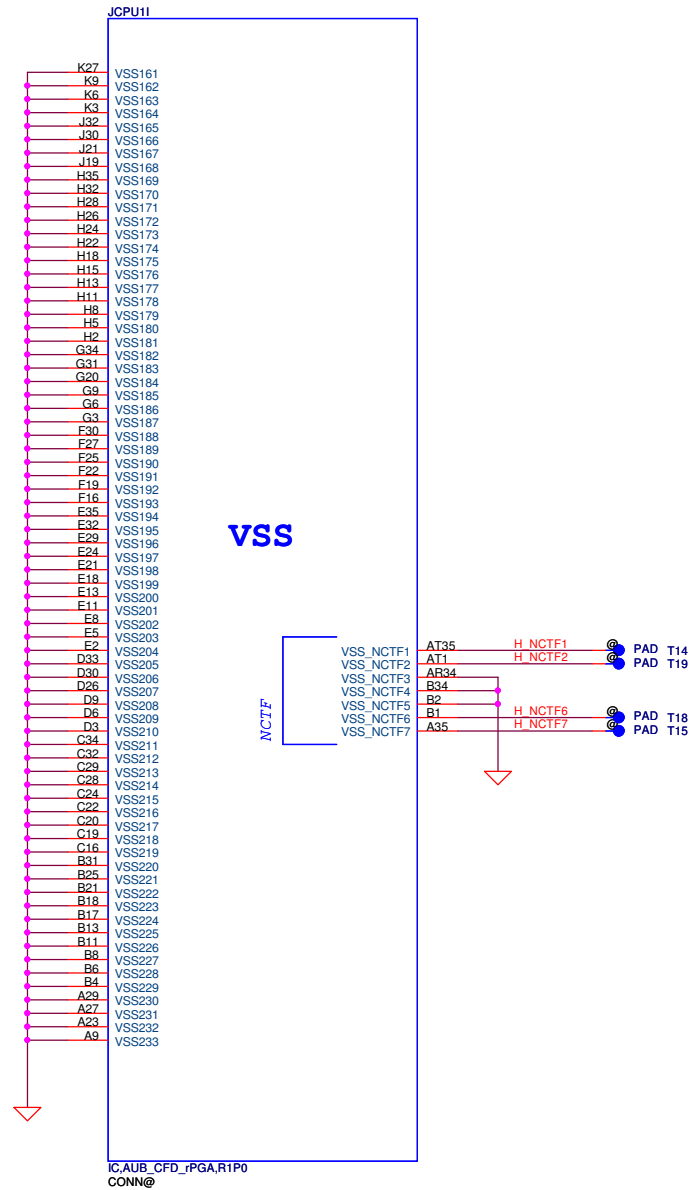
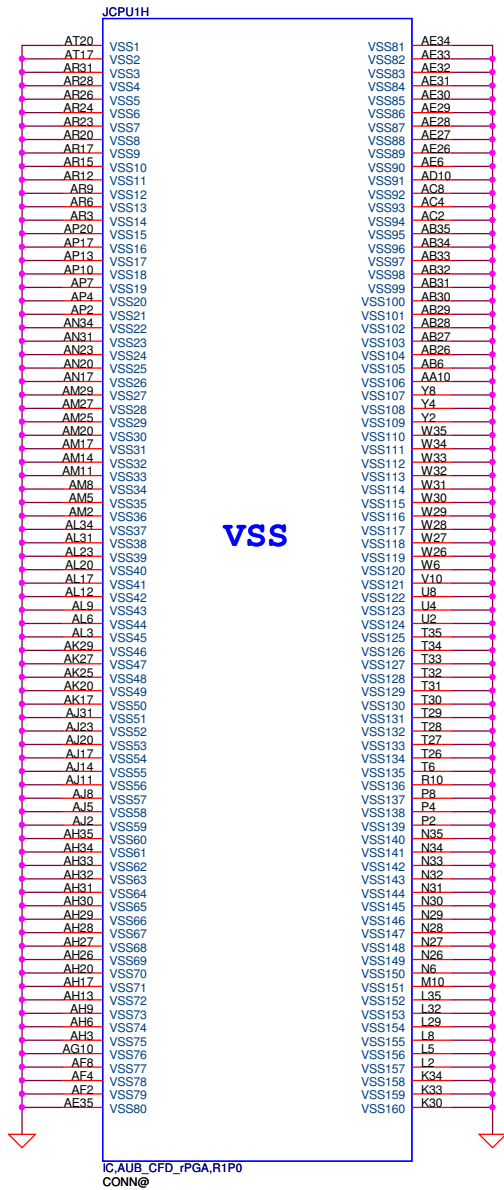
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						Size B		Document Number		Rev 1.0	
						NEW70 M/B LA-5891P Schematic					
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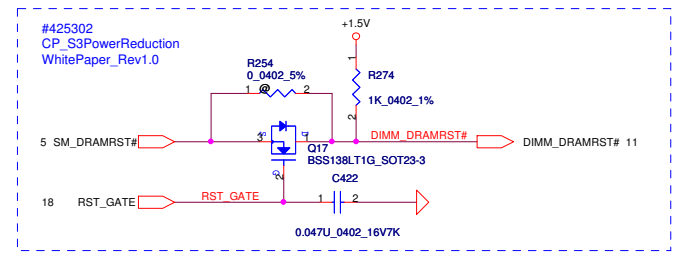
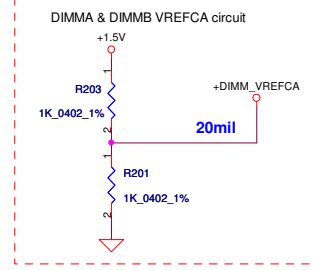
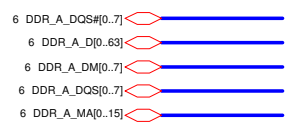
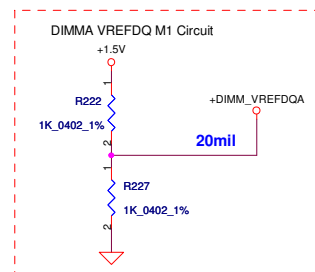


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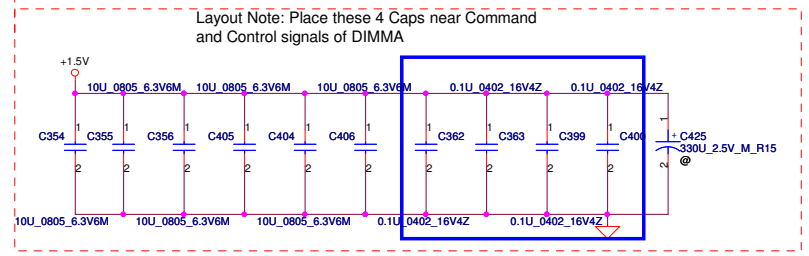




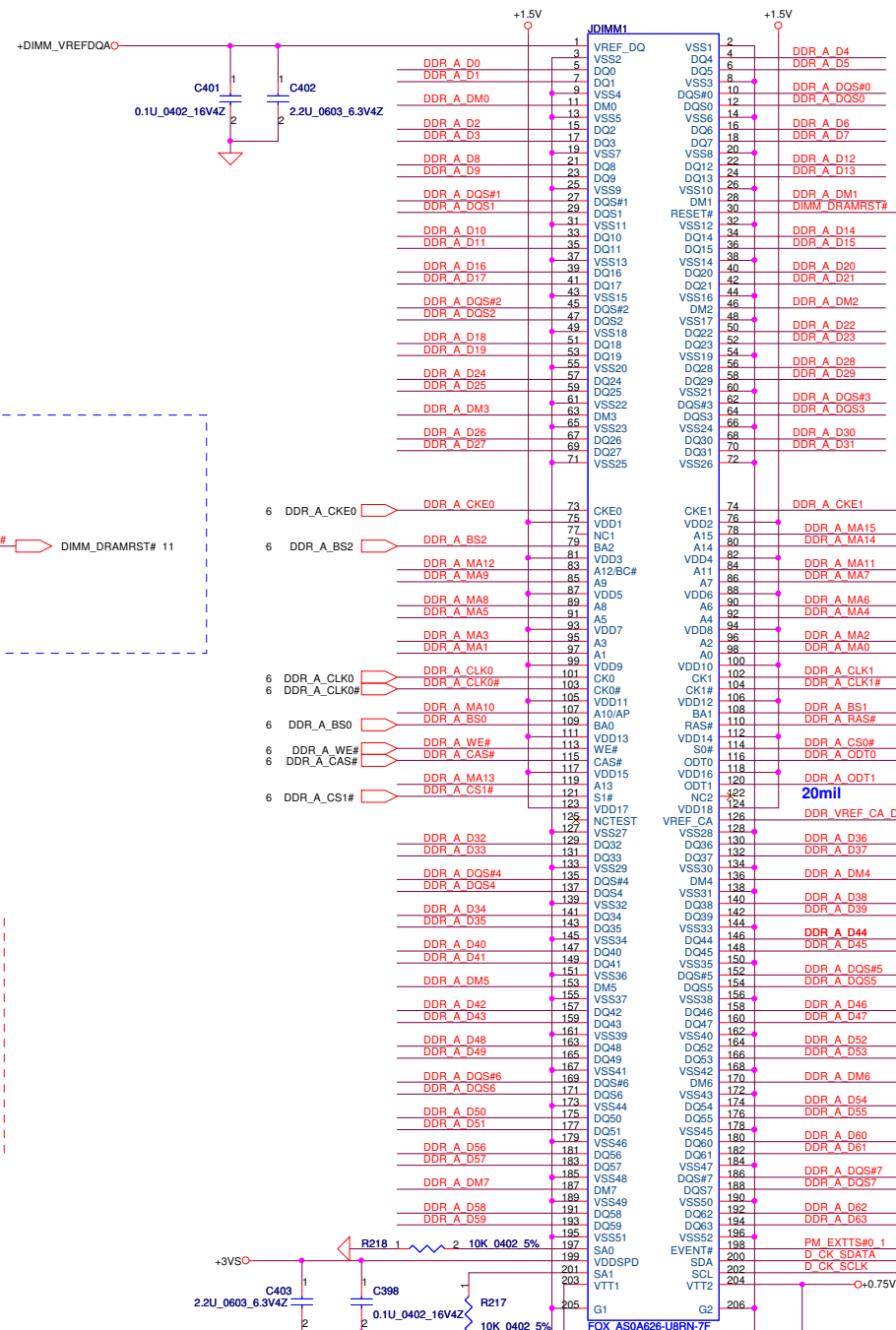
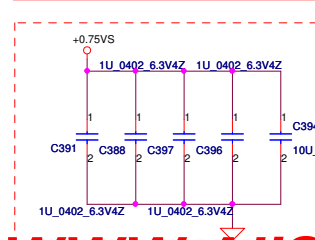
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						Customer	NEW70 M/B LA-5891P Schematic			1.0	
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**Layout Note:**  
Place near JDIMM1

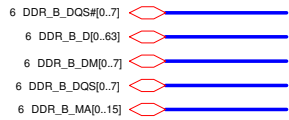


**Layout Note:**  
Place near JDIMM1.203 & JDIMM1.204

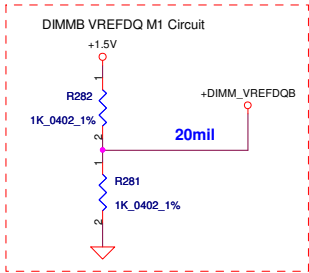
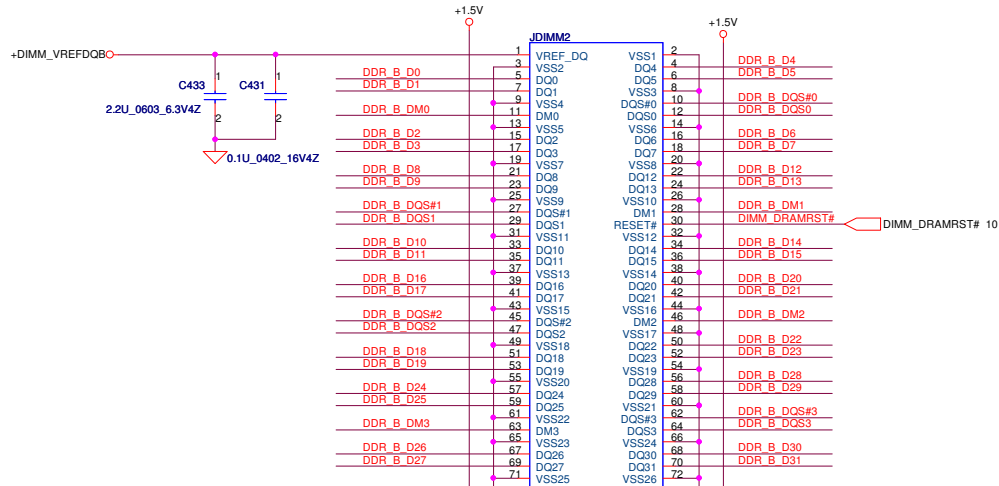


**DDR3 SO-DIMM A  
H=8mm**

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				Rev	1.0				
				Date	Tuesday, December 29, 2009	Sheet	10	of	59

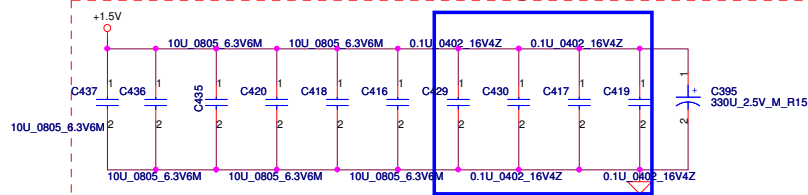


2008/9/8 #400755  
Calpella Clarkfield  
DDR3 SO-DIMM  
VREFDQ Platform  
Design Guide Change Details

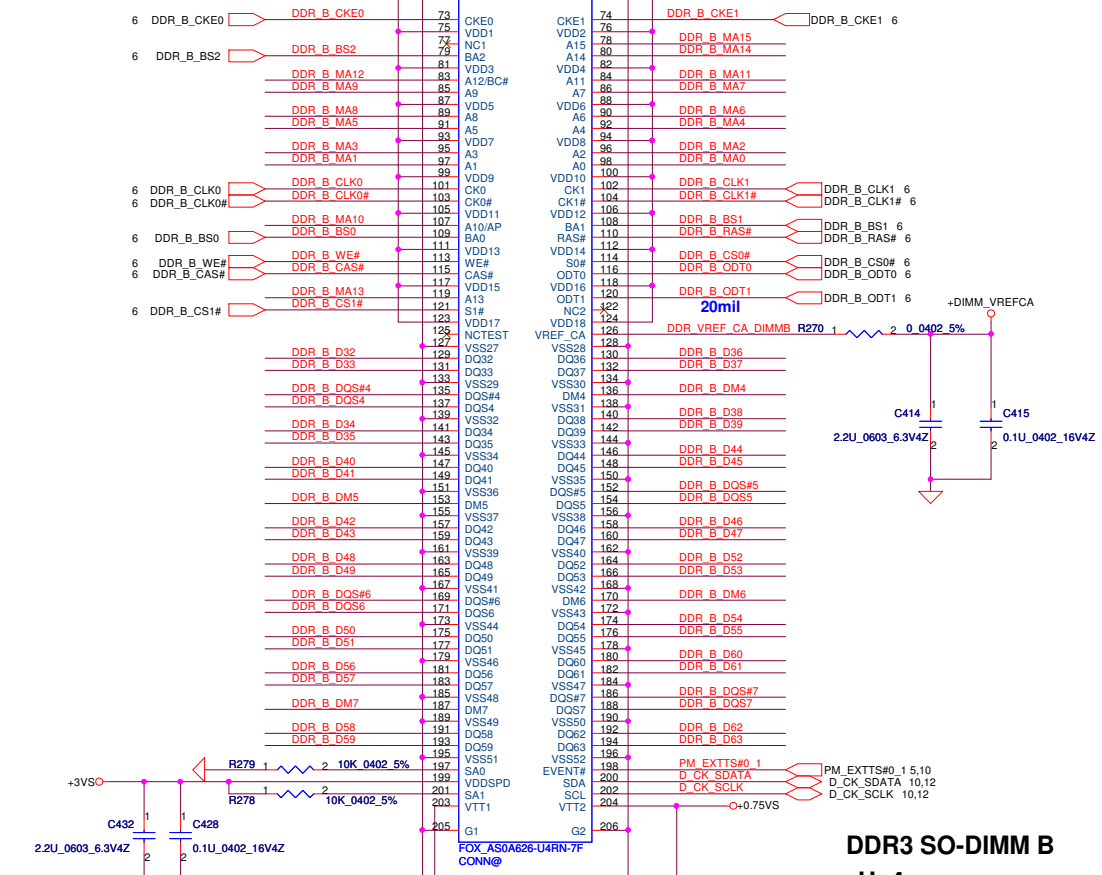
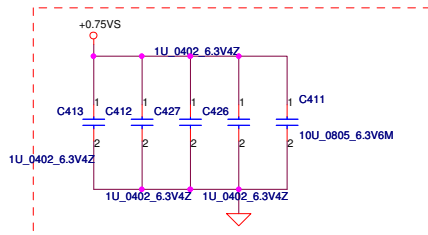


Layout Note:  
Place near JDIMM2

Layout Note: Place these 4 Caps near Command  
and Control signals of DIMMB

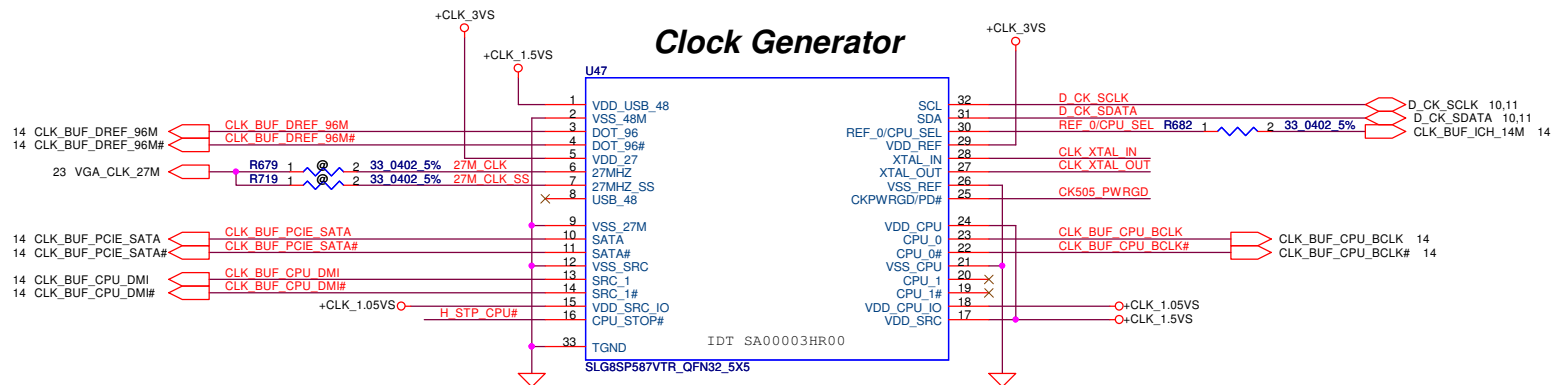
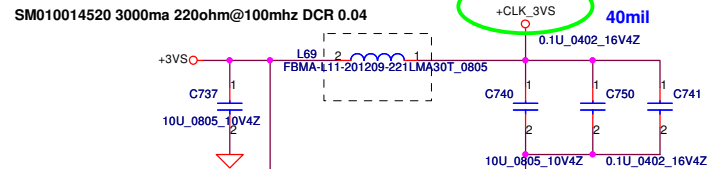


Layout Note:  
Place near JDIMM2.203 & JDIMM2.204



DDR3 SO-DIMM B  
H=4mm

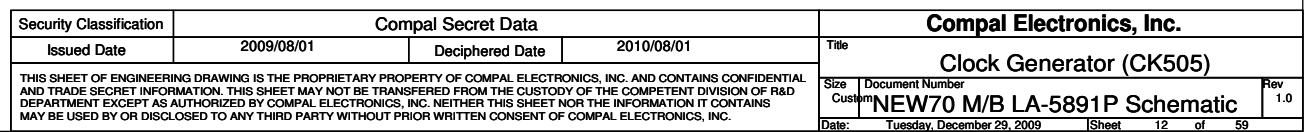
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				NEW70 M/B LA-5891P Schematic	
				Date	Rev
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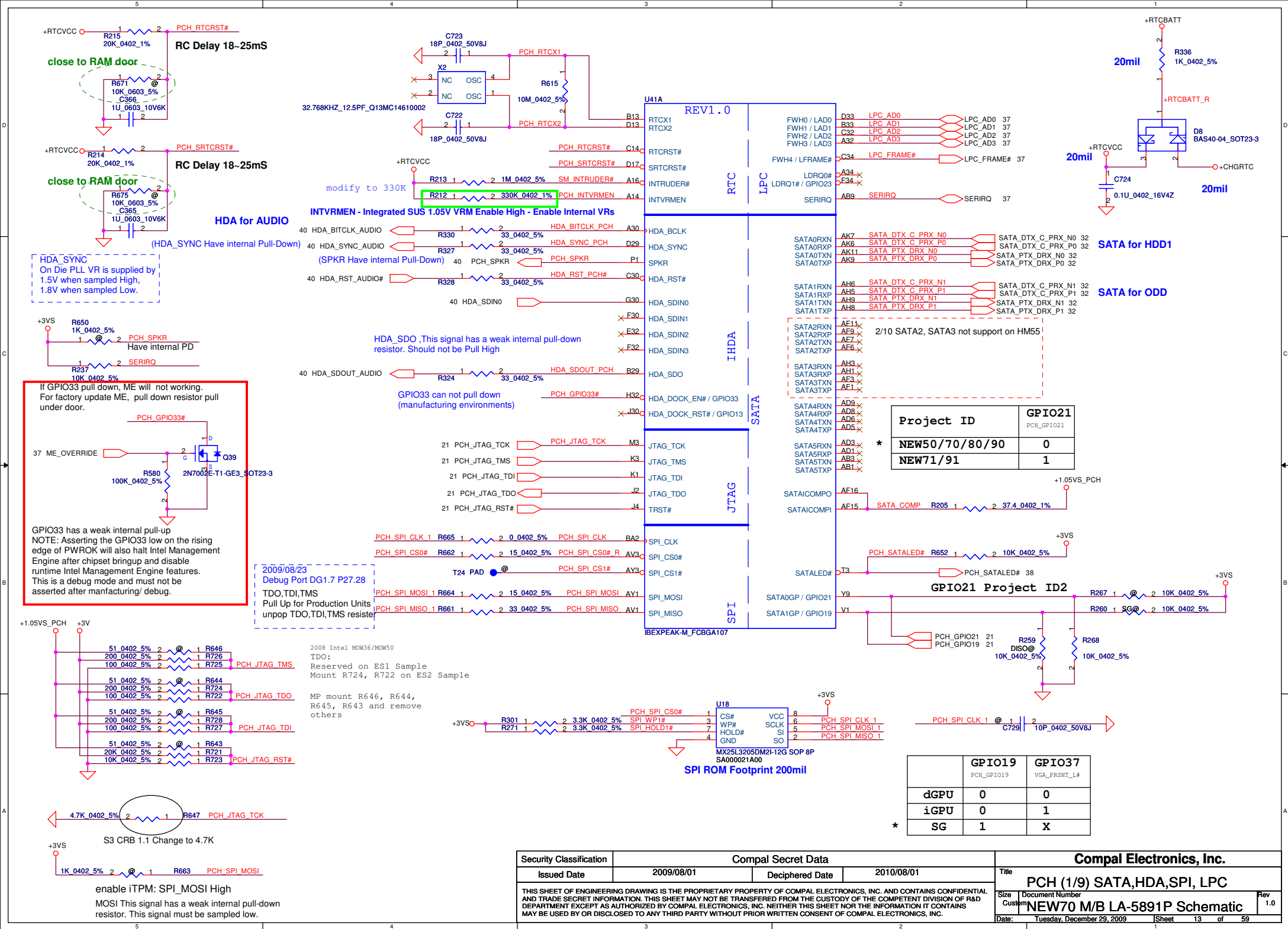


**Silego Have Internal Pull-Up**

The diagram shows a circuit connection. A +3V supply is connected to pin 1 of an R690 component. Pin 2 of the R690 is connected to a 10K 0402 5% resistor. The other end of the resistor is connected to pin H of an STP CPU# component.

R683 1 2 10K 0402 5% REF 0/CPU SEL





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For PCIE LAN

For Wireless LAN

For Mini2

For PCIE LAN

For Wireless LAN

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS
3. Level Shift2, Pull-Up to +3VS
4. Level Shift3, Pull-Up to +3VS

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

Change to 5x3.2

U41B REV1.0

PCI-E\*

From CLK BUFFER

Clock Flex

1222 GPIO66  
PULL HIGH:8L  
PULL DOWN:6L

### Project Structure

GPIO21	GPIO65	GPIO66	Structure
ID2	ID1	ID0	
0	0	0	DVT
0	0	1	
0	1	0	PVT

Security Classification

Compal Secret Data

Issued Date

2009/08/01

Deciphered Date

2010/08/01

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Compal Electronics, Inc.

Title

PCH (2/9) PCIE, SMBUS, CLK

Size

Document Number

NEW70 M/B LA-5891P Schematic

Rev

1.0

Date

Friday, January 08, 2010

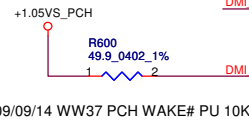
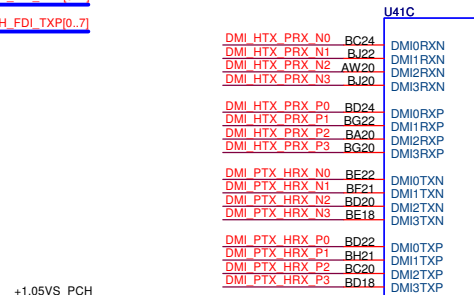
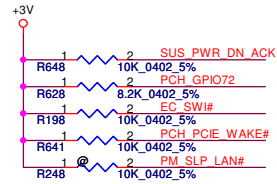
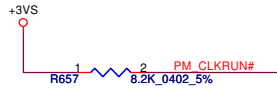
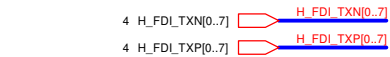
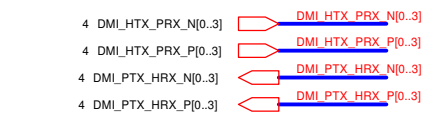
Sheet

14

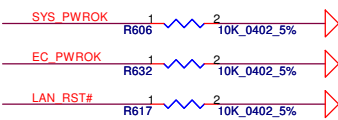
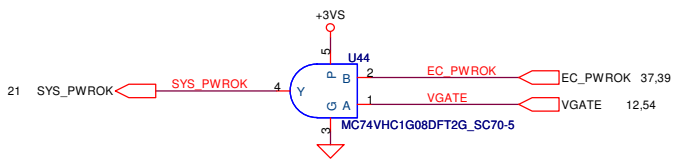
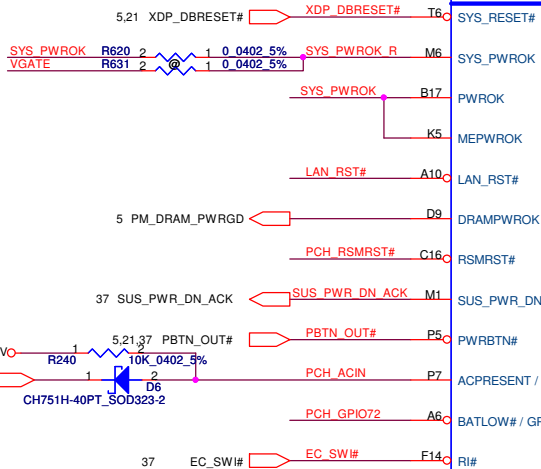
of

59



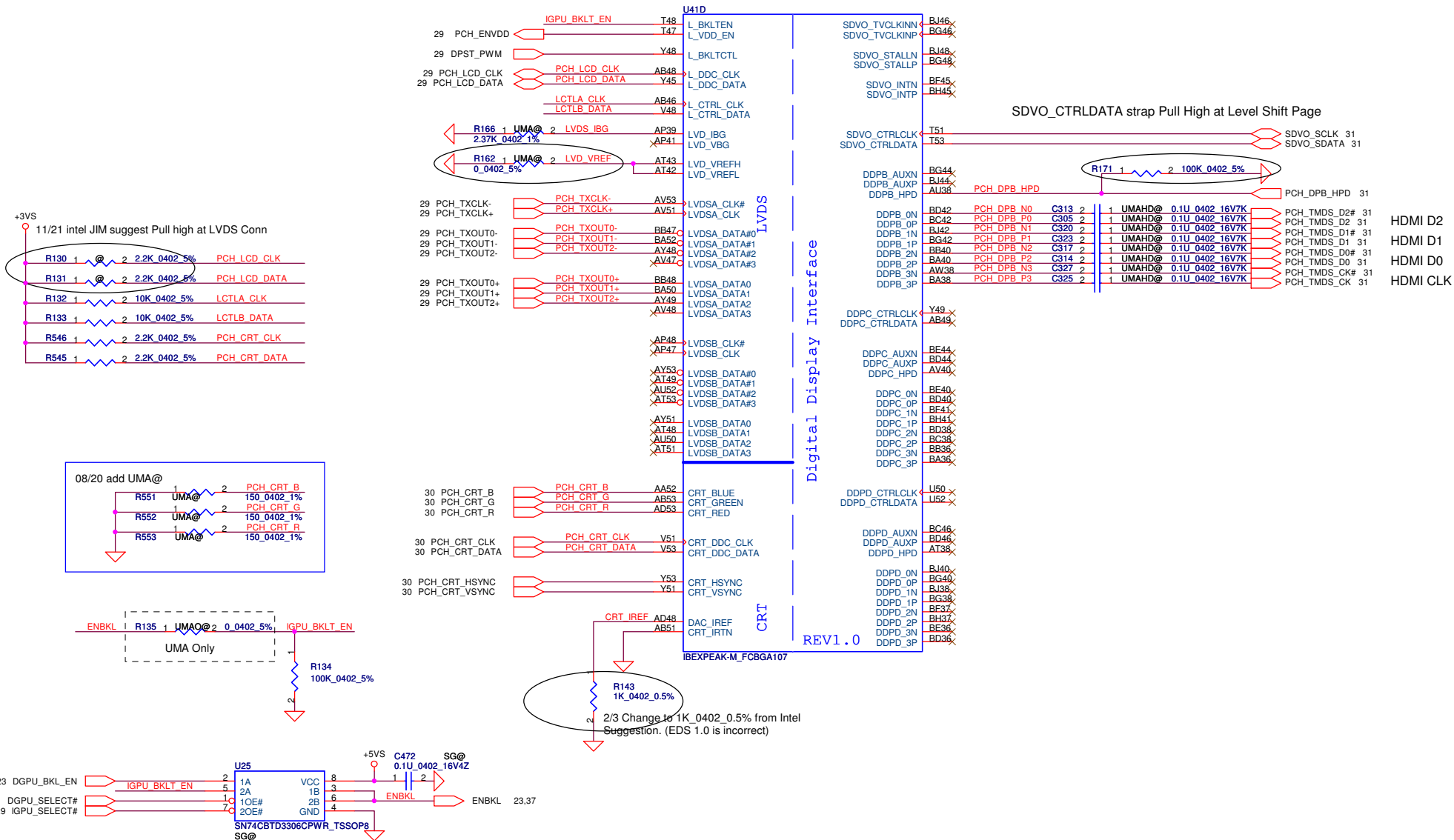


09/09/14 WW37 PCH WAKE# PU 10K

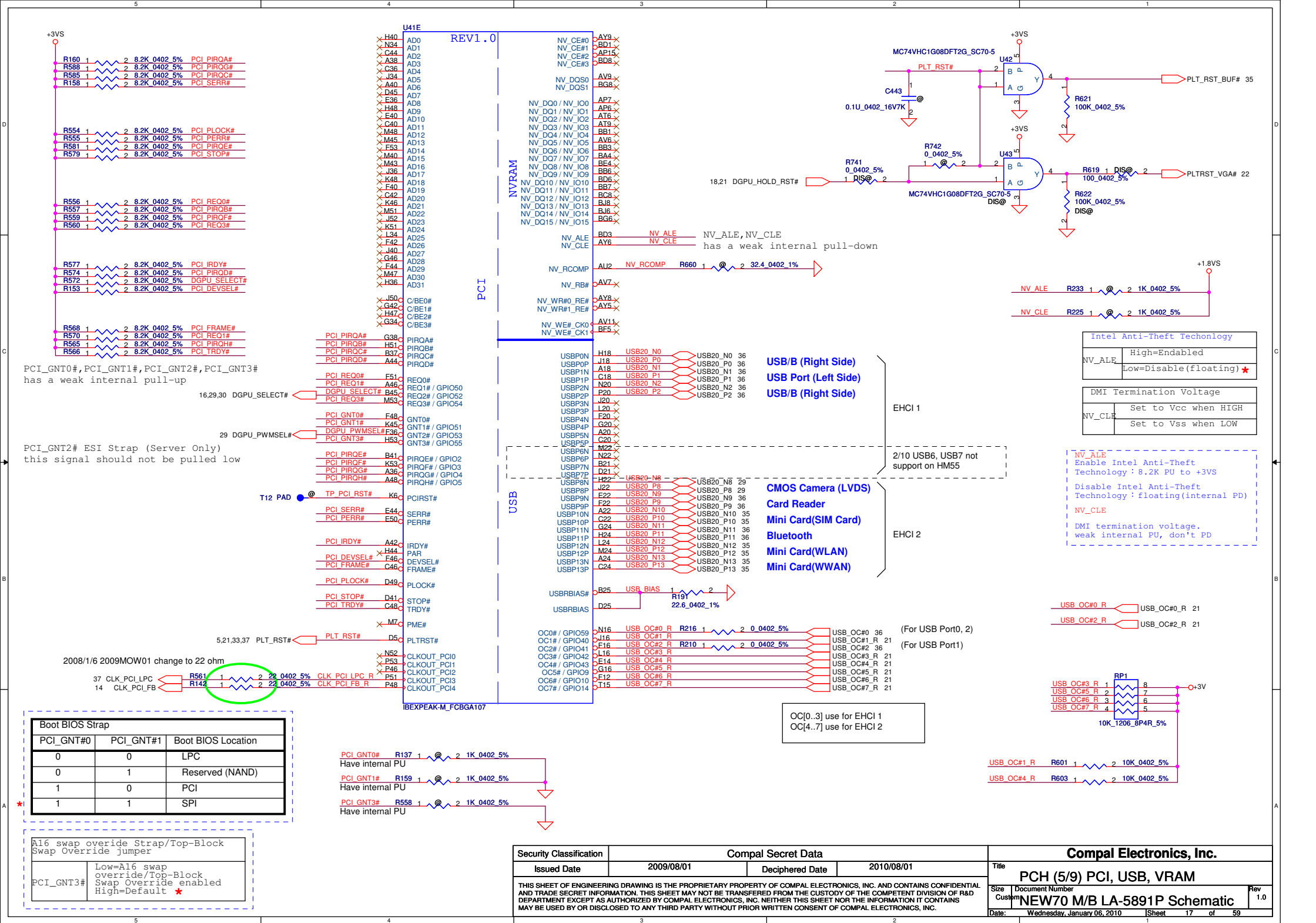


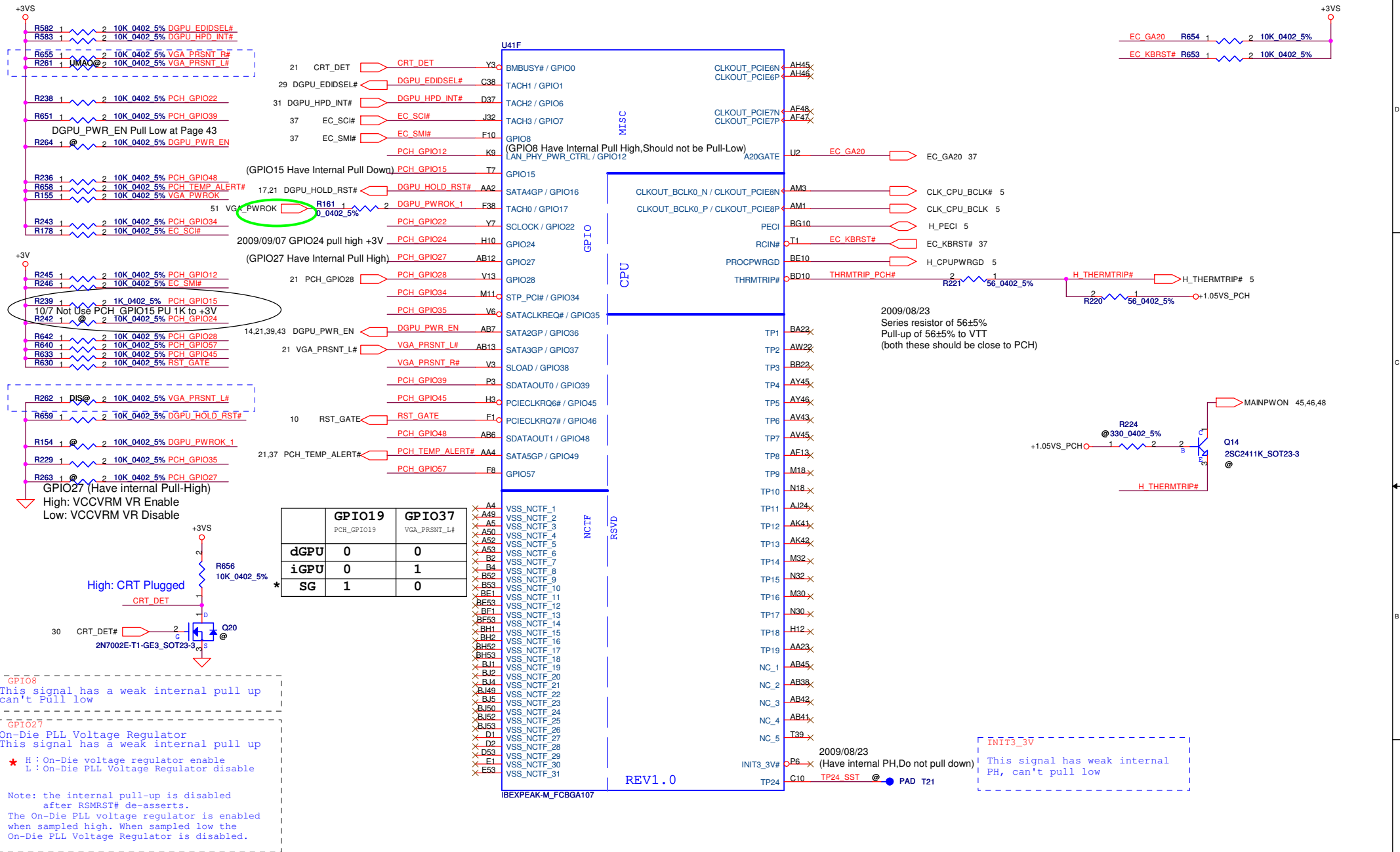
No used Integrated LAN,  
connecting LAN\_RST# to GND

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Size	Custom	Document Number	NEW70 M/B LA-5891P Schematic	Rev	1.0
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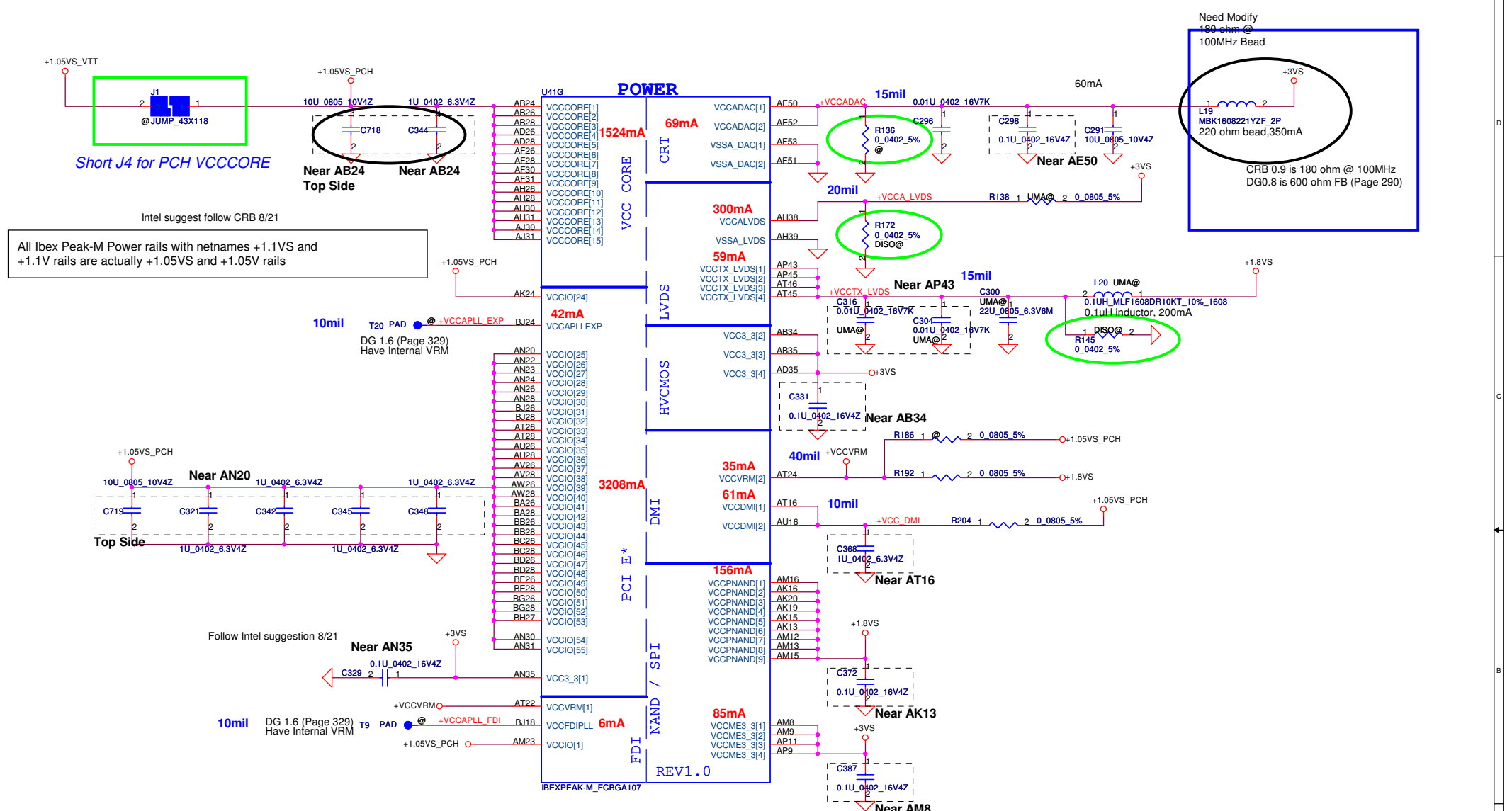


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Need Modify  
180 ohm @  
100MHz Bead

L19  
MBK1608221YZF\_2P  
220 ohm bead,350mA

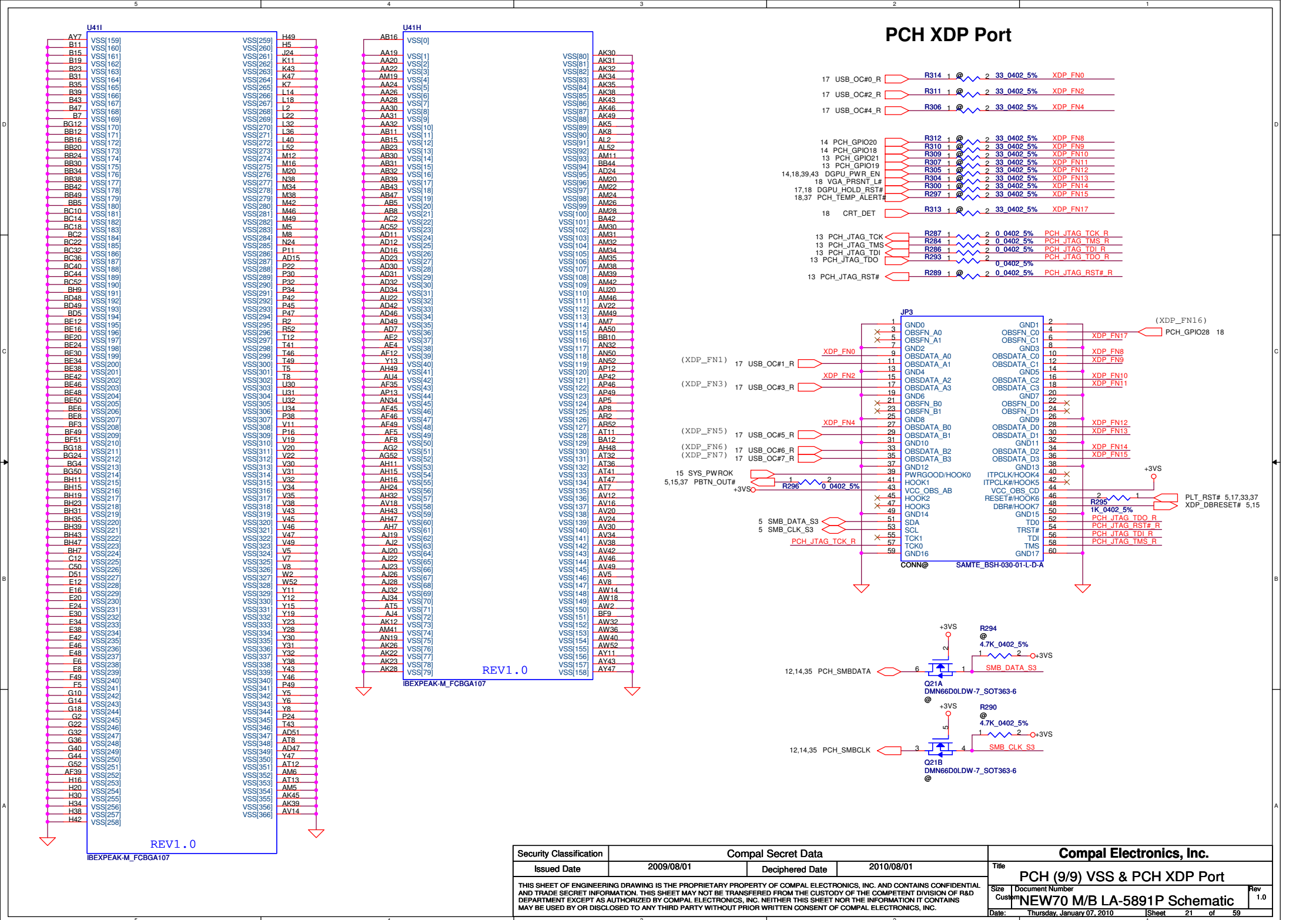
CRB 0.9 is 180 ohm @ 100MHz  
DG0.8 is 600 ohm FB (Page 290)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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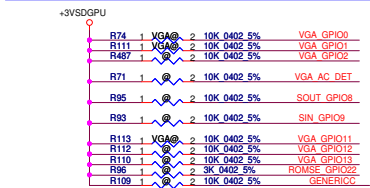
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	PCH (8/9) PWR	
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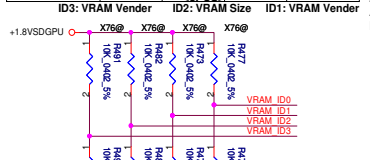


Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the memory apertures CONFIG[3:0] 128 MB 001 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	Advertises the PCIe device as 2.5 GT/s capable at power-on 1: Advertises the PCIe device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	

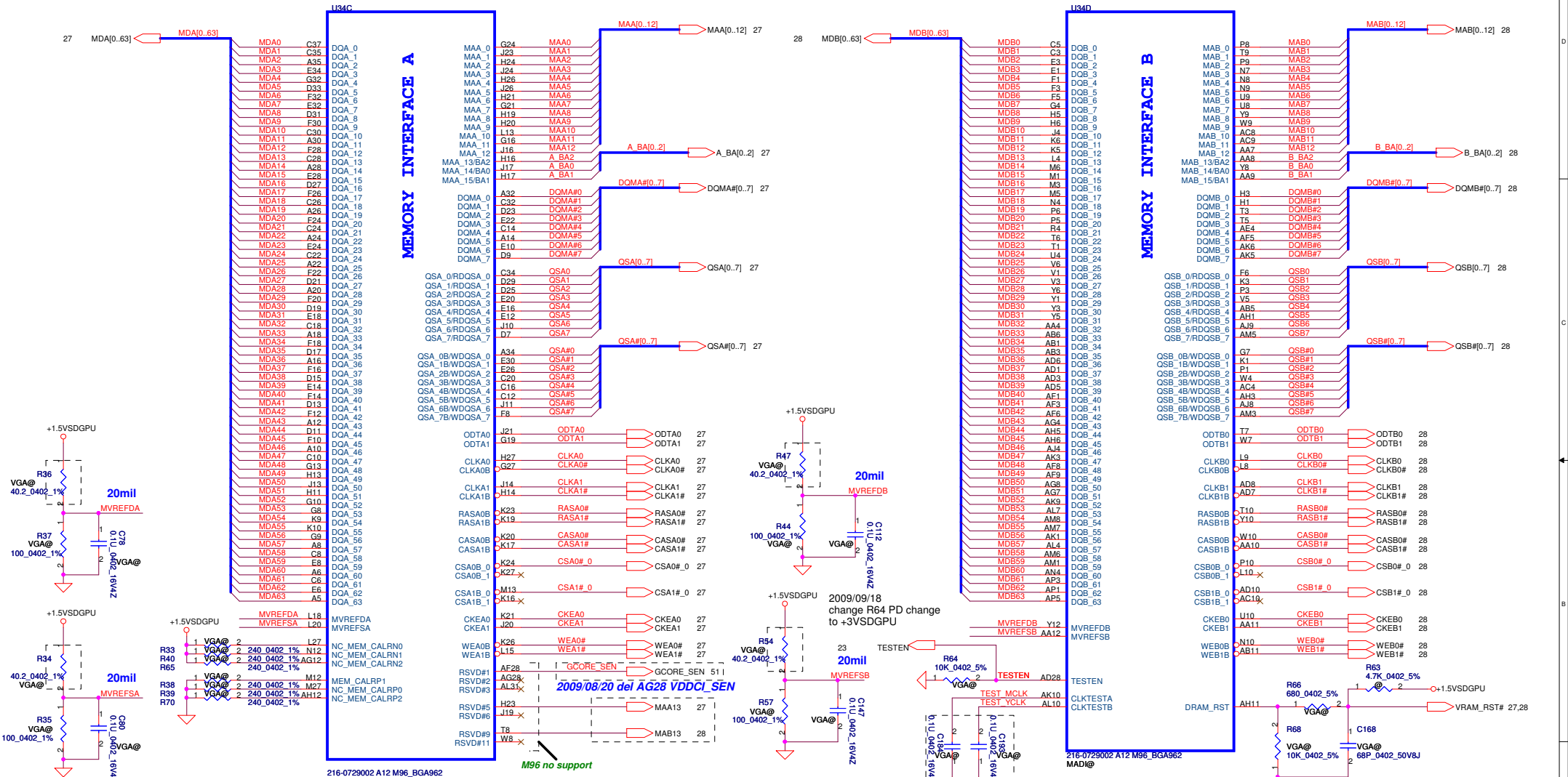


Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	64Mx16	64Mx16	0	0
HYNIX	1	<4PCS>	0	0
AMD	1	<4PCS>	1	0

Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	64Mx16	64Mx16	0	0
HYNIX	1	<4PCS>	0	0
AMD	1	<4PCS>	1	0



Park is single channel for memory (channel B only)



If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

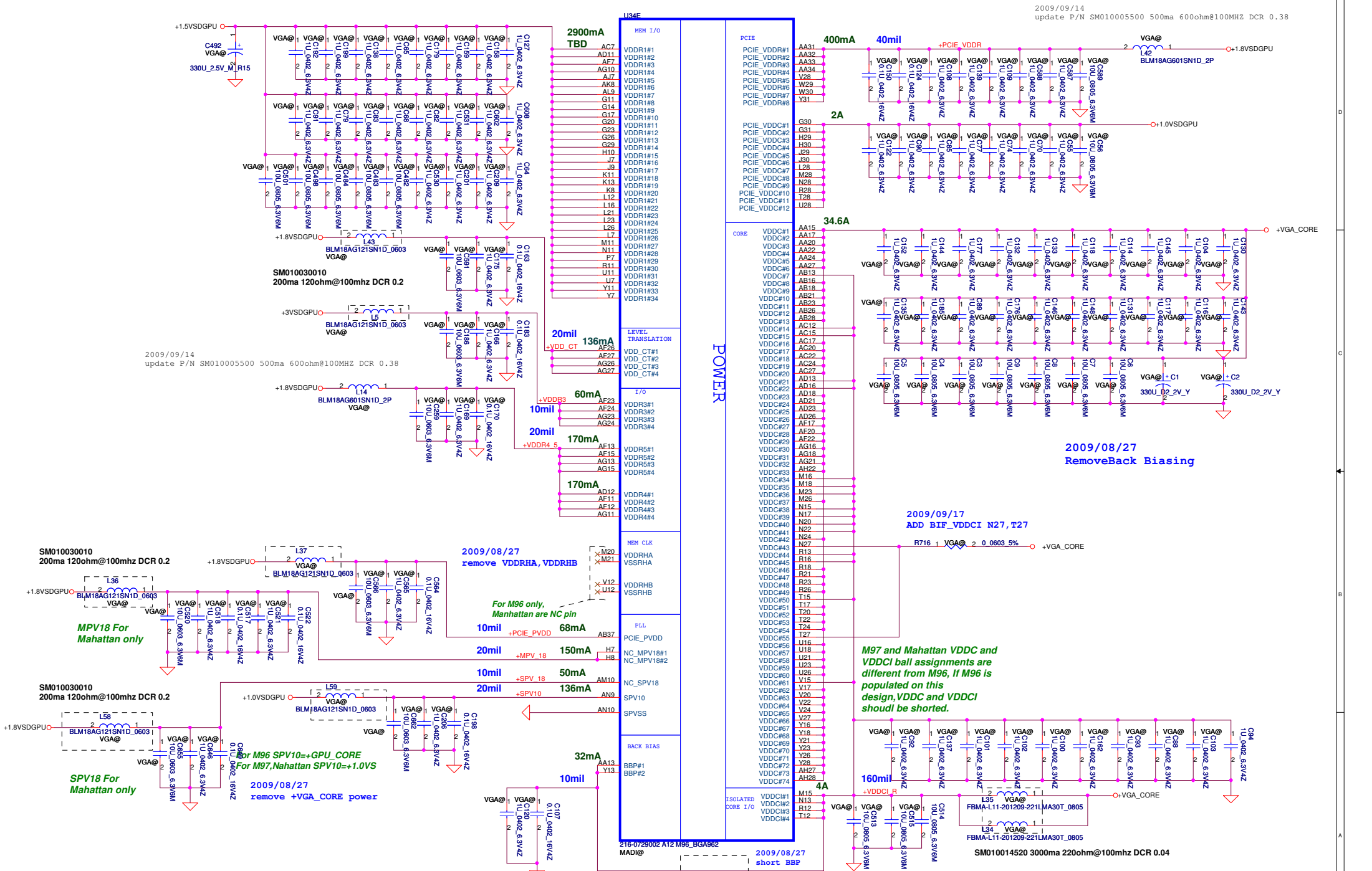
In M97, Medison and Park, AF28 is FB\_VDDC, AG28 is FB\_VDDCI, AH29 is FB\_GND. GCORE\_SEN and FB\_GND should route as differential pair Same as VDDCI\_SEN and FB\_GND

If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

M96 use 4.7K to PD directly.

	M96	Broadway
R228	4.7k Ohm	10k Ohm
R159	SD028470180	SD028100280
R159	SD02800080	SD028680080
R159	SD028470180	SD028470180
C659	1000 pf	68 pf
C659	SD074102K80	SD071680J80

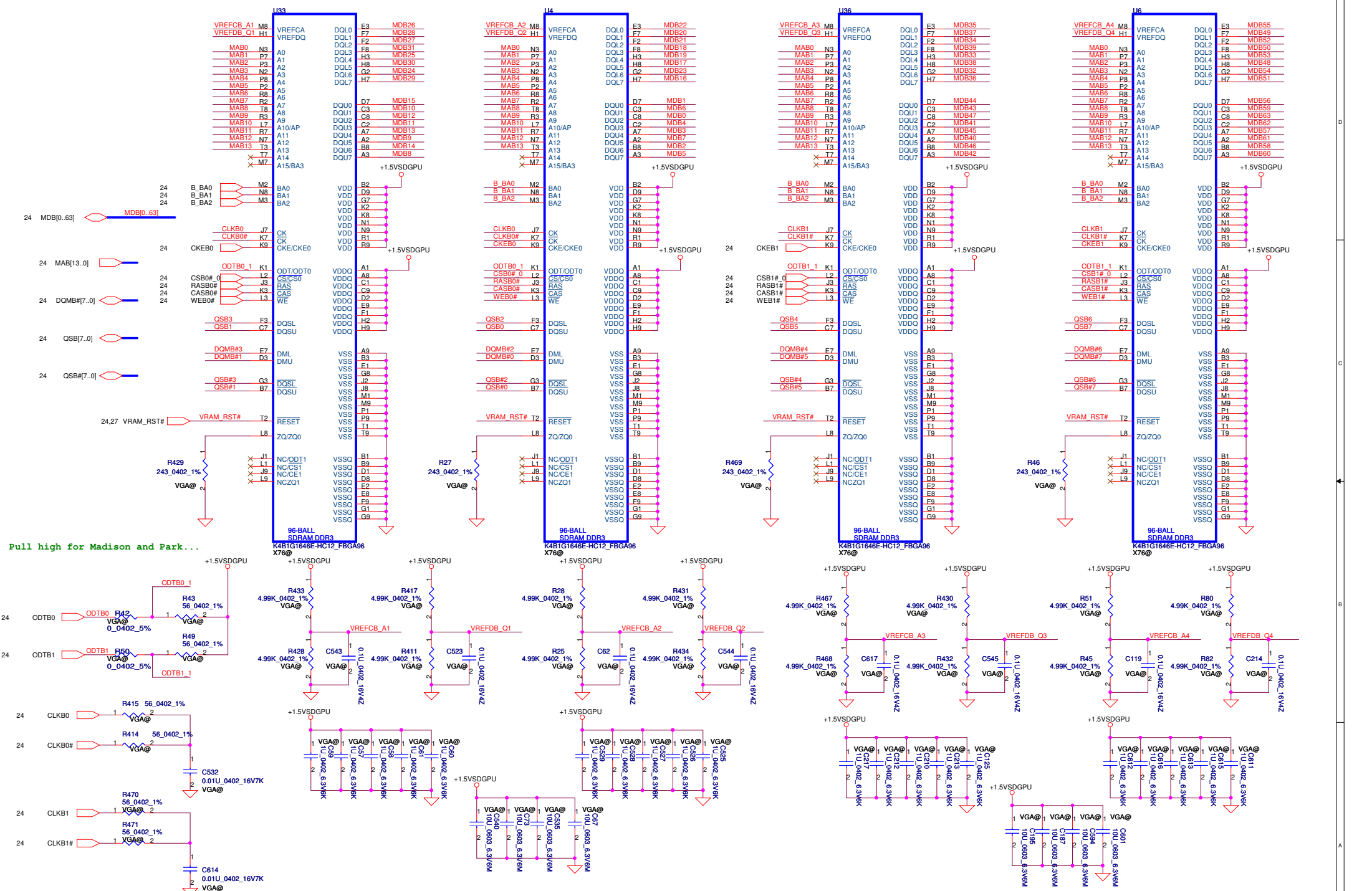




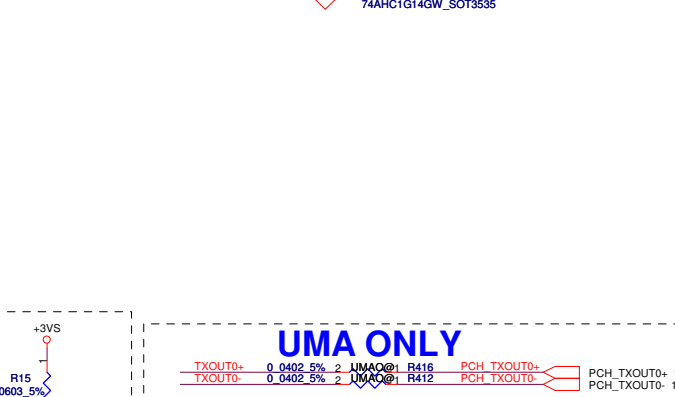
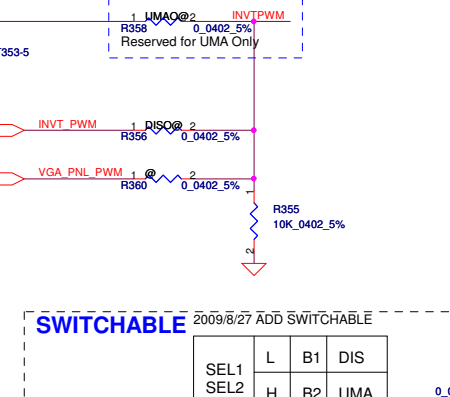
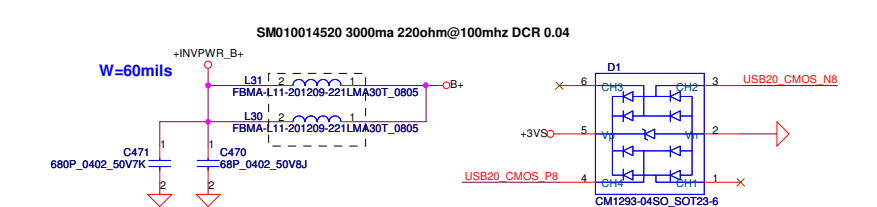
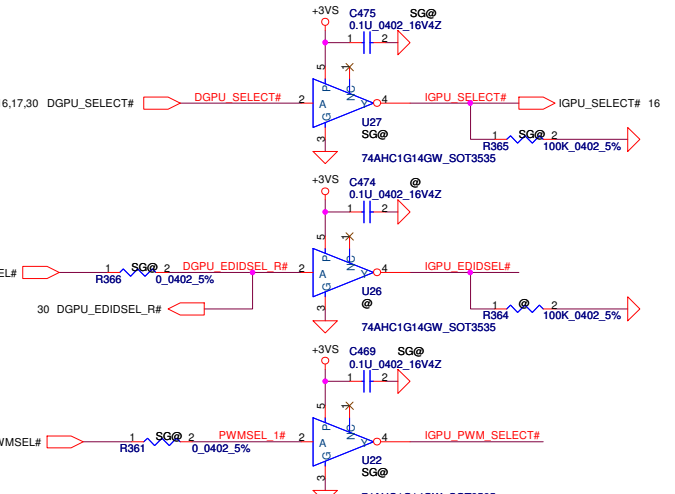
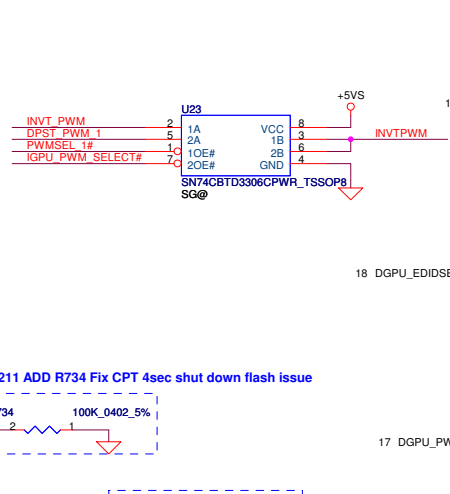
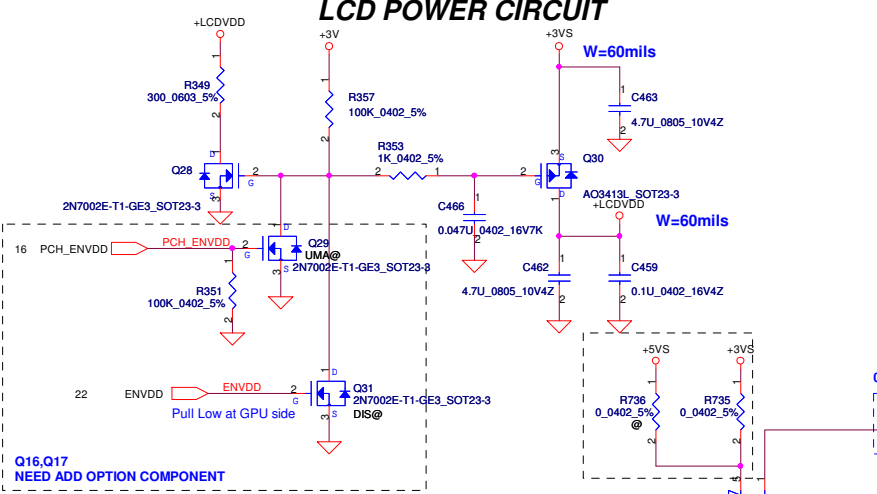




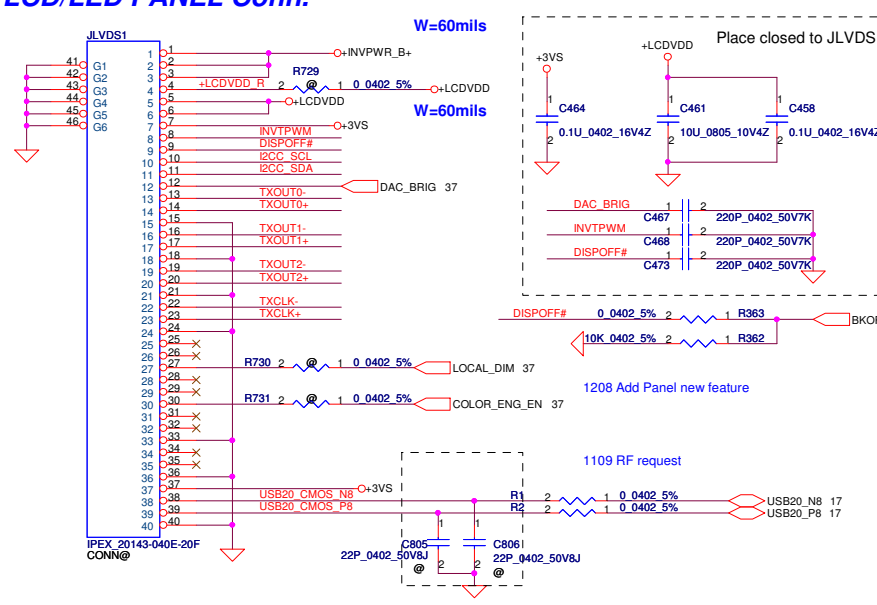




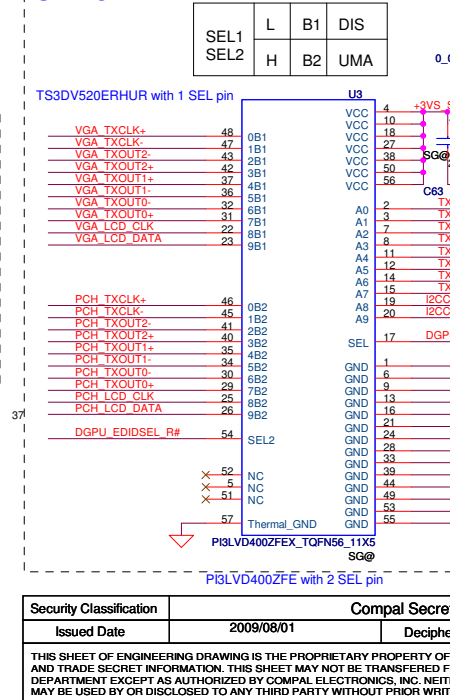
# LCD POWER CIRCUIT



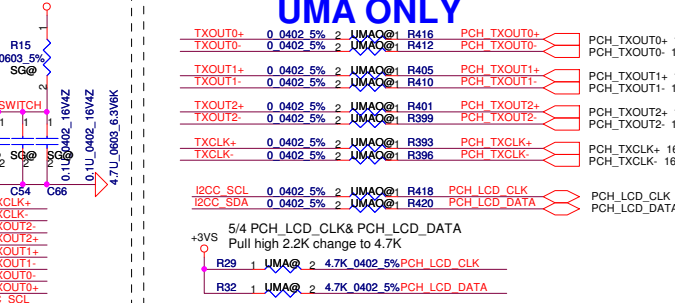
## LCD/LED PANEL Conn.



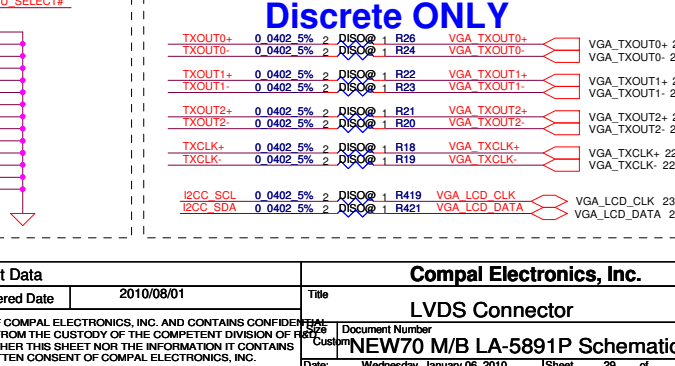
## SWITCHABLE



## UMA ONLY

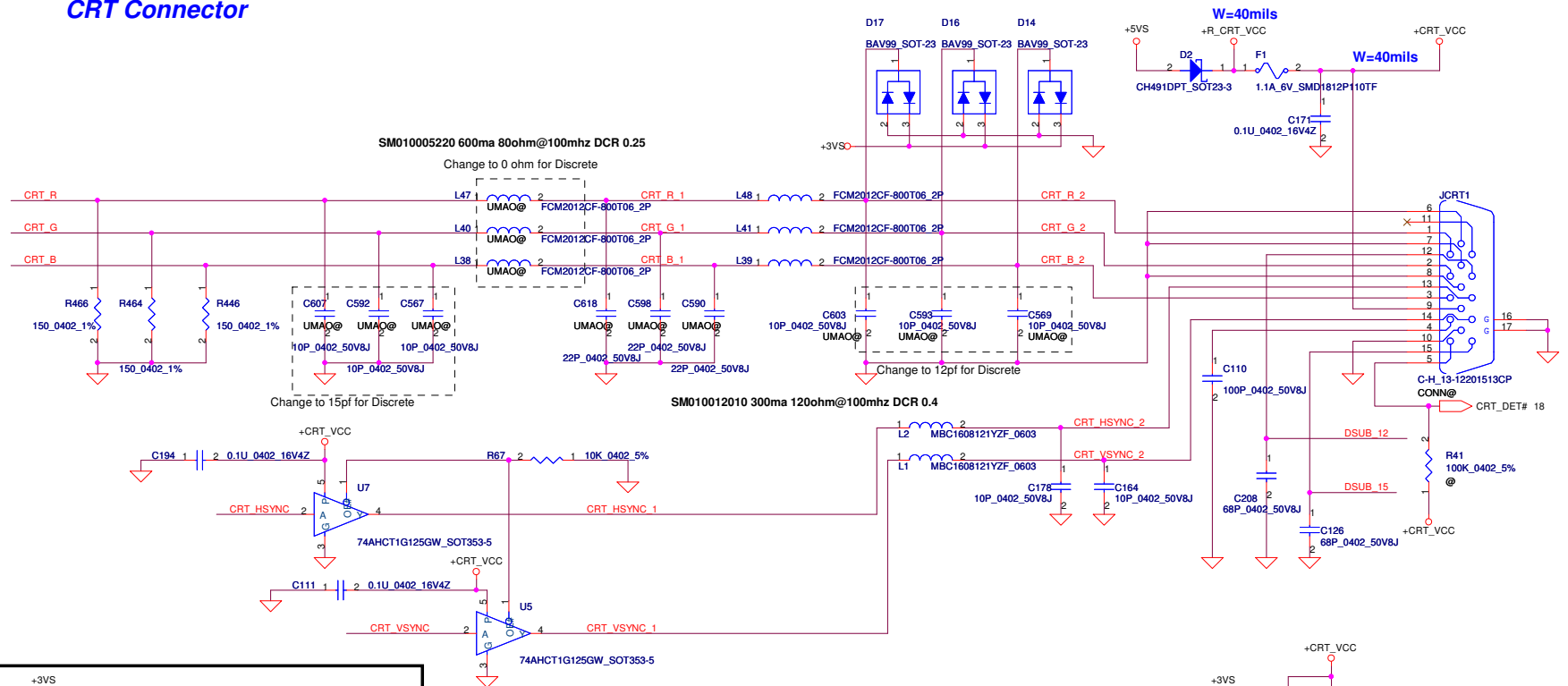


## Discrete ONLY



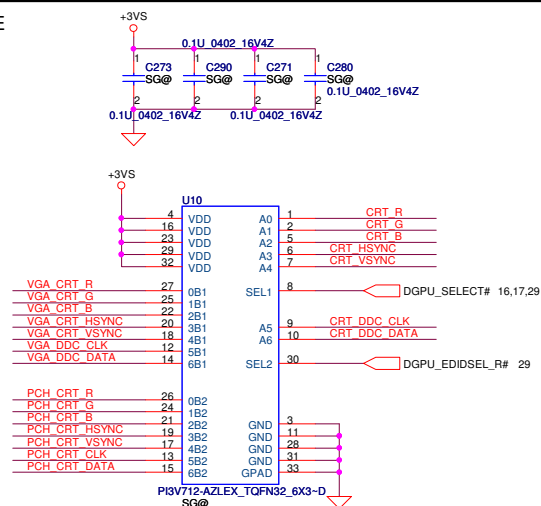
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# CRT Connector



## SWITCHABLE

2009/08/27



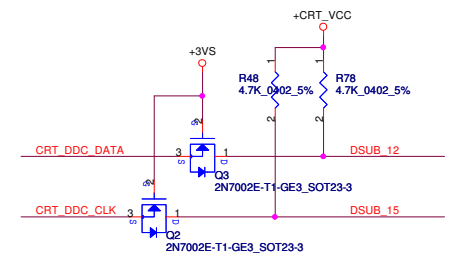
L	B1	DIS
H	B2	UMA

## UMA only

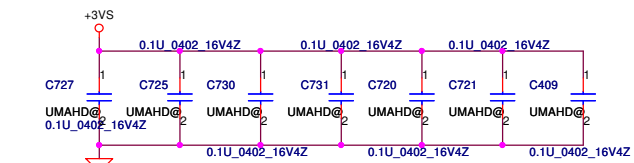
16 PCH_CRT_R	PCH CRT R	R536	2	UMA0	1	0.0402 5%	CRT_R
16 PCH_CRT_G	PCH CRT G	R534	2	UMA0	1	0.0402 5%	CRT_G
16 PCH_CRT_B	PCH CRT B	R532	2	UMA0	1	0.0402 5%	CRT_B
16 PCH_CRT_HSYNC	PCH CRT HSYNC	R530	2	UMA0	1	0.0402 5%	CRT_HSYNC
16 PCH_CRT_VSYNC	PCH CRT VSYNC	R528	2	UMA0	1	0.0402 5%	CRT_VSYNC
16 PCH_CRT_CLK	PCH CRT CLK	R544	2	UMA0	1	0.0402 5%	CRT_DDC_CLK
16 PCH_CRT_DATA	PCH CRT DATA	R543	2	UMA0	1	0.0402 5%	CRT_DDC_DATA

## Discrete only

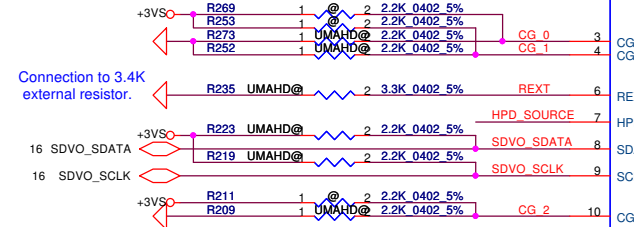
23 VGA_CRT_R	VGA CRT R	R537	2	DIS00	1	0.0402 5%	CRT_R
23 VGA_CRT_G	VGA CRT G	R535	2	DIS00	1	0.0402 5%	CRT_G
23 VGA_CRT_B	VGA CRT B	R533	2	DIS00	1	0.0402 5%	CRT_B
23 VGA_CRT_HSYNC	VGA CRT HSYNC	R531	2	DIS00	1	0.0402 5%	CRT_HSYNC
23 VGA_CRT_VSYNC	VGA CRT VSYNC	R529	2	DIS00	1	0.0402 5%	CRT_VSYNC
23 VGA_DDC_CLK	VGA DDC CLK	R527	2	DIS00	1	0.0402 5%	CRT_DDC_CLK
23 VGA_DDC_DATA	VGA DDC DATA	R526	2	DIS00	1	0.0402 5%	CRT_DDC_DATA



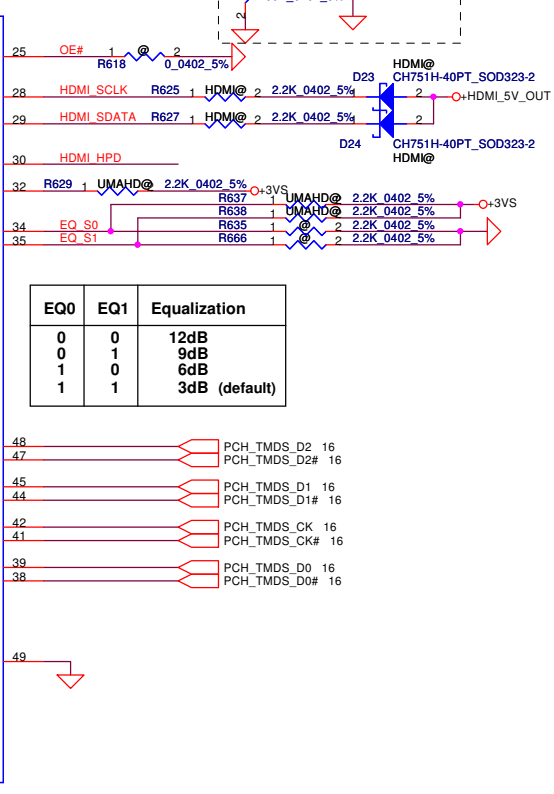
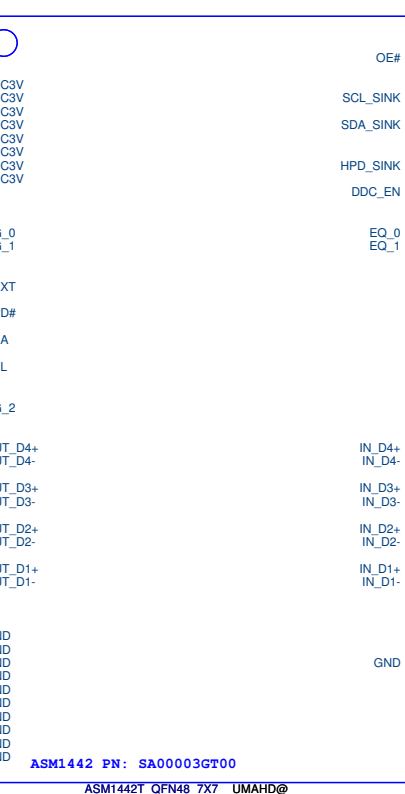
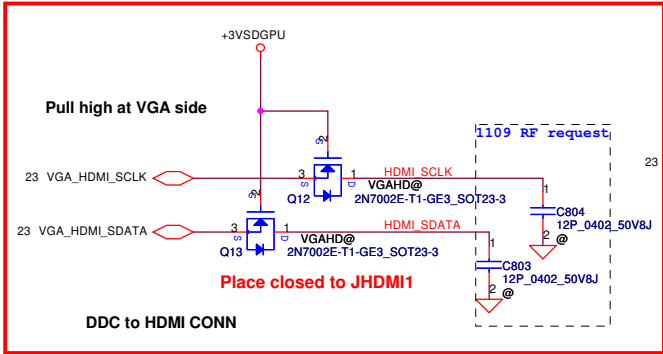
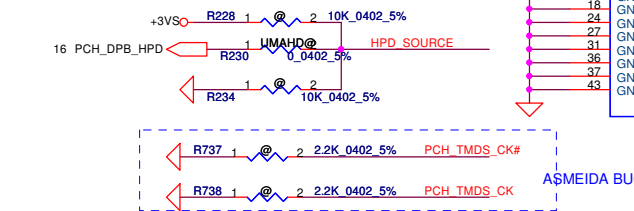
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Date		Document Number NEW70 M/B LA-5891P Schematic	Rev 1.0
Tuesday, December 29, 2009		Sheet	30 of 59



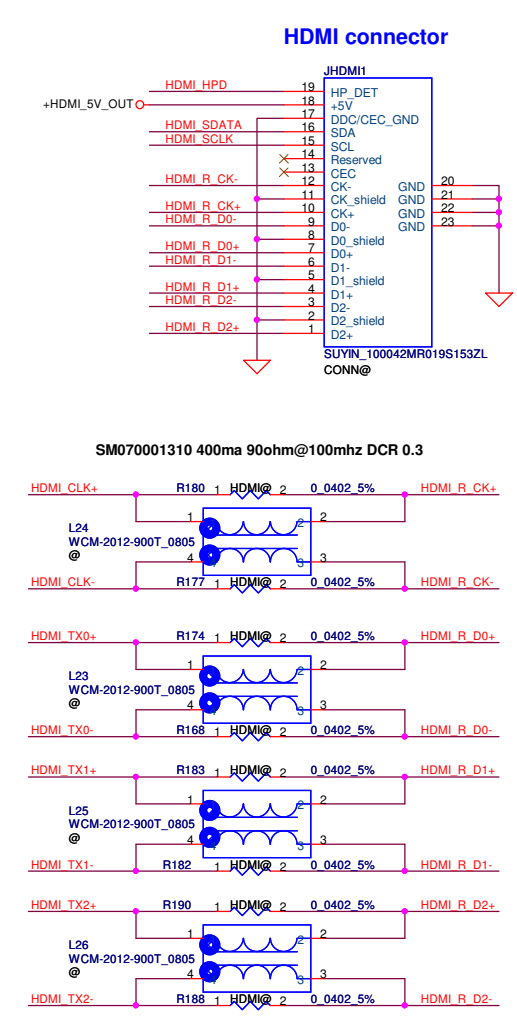
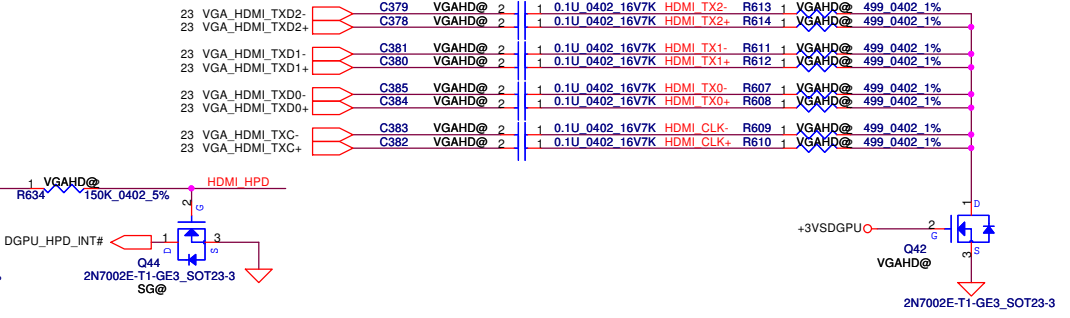
Option	UMAHD@	VGAHD@	HDMI@	@	SG@
UMA	V	X	V	X	X
VGA	X	V	V	X	X
SG	X	V	V	X	V
NO HDMI	X	X	X	X	X



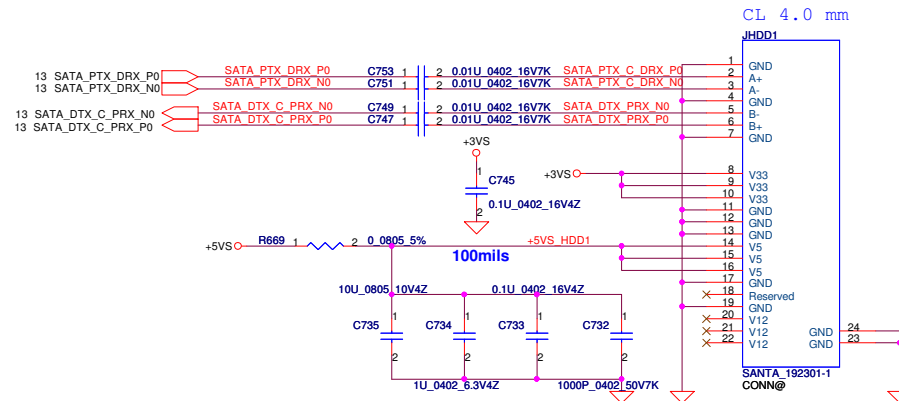
CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0



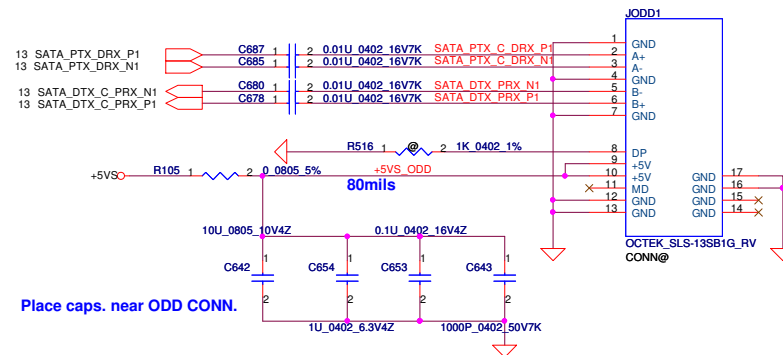
EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)



**SATA HDD1 Conn.**

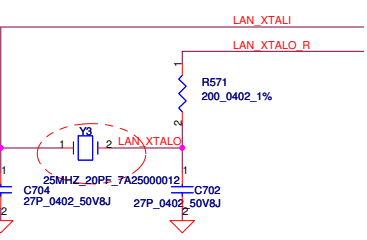


**SATA ODD Conn.**



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				NEW70 M/B LA-5891P Schematic	
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**LAN Section Schematic**

**Power and Ground Connections:**

- +3V\_LAN:** Connected to the VCC pin (pin 8) of the AT24C02\_S08 IC.
- +1.2V\_LAN:** Connected to the A0 pin (pin 1) of the AT24C02\_S08 IC.
- GND:** Connected to the GND pin (pin 4) of the AT24C02\_S08 IC.

**Signal Connections:**

- SPROM\_CLK:** Connected to the SCL pin (pin 6) of the AT24C02\_S08 IC.
- SPROM\_DOUT:** Connected to the SDA pin (pin 5) of the AT24C02\_S08 IC.

**Internal Components:**

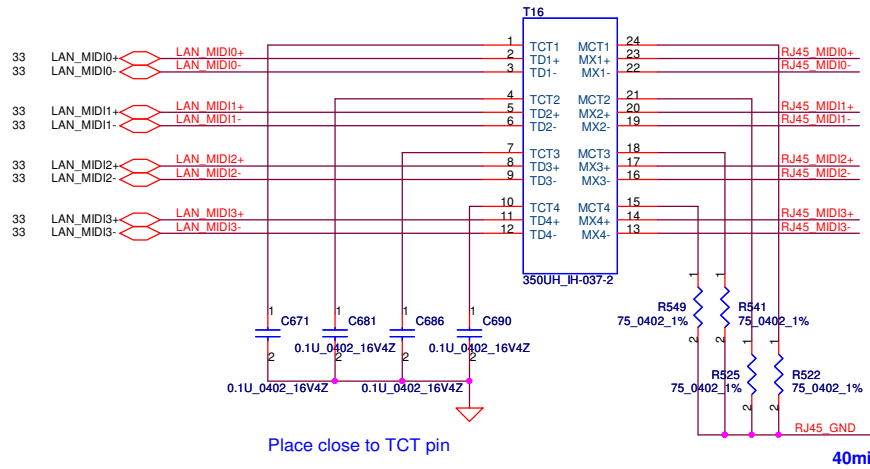
- Resistors:** R195 (1K\_0402\_1%), R193 (1K\_0402\_1%), R196 (1K\_0402\_1%), R194 (1K\_0402\_1%).
- Capacitors:** C301 (0.1U\_0402\_16V4Z), C703 (0.1U\_0402\_16V4Z), C712 (0.1U\_0402\_16V4Z), C706 (0.1U\_0402\_16V4Z), C302 (0.1U\_0402\_16V4Z), C695 (4.7U\_0603\_6.3V6K), C696 (4.7U\_0603\_6.3V6K), C709 (0.1U\_0402\_16V4Z), C312 (4.7U\_0603\_6.3V6K).
- Inductors:** L22 (BLM18AG601SN1D\_2P), L64 (BLM18AG601SN1D\_2P), L66 (BLM18AG601SN1D\_2P), L83 (BLM18AG601SN1D\_2P), L62 (BLM18AG601SN1D\_2P), L21 (BLM18AG601SN1D\_2P).

**Module Information:**

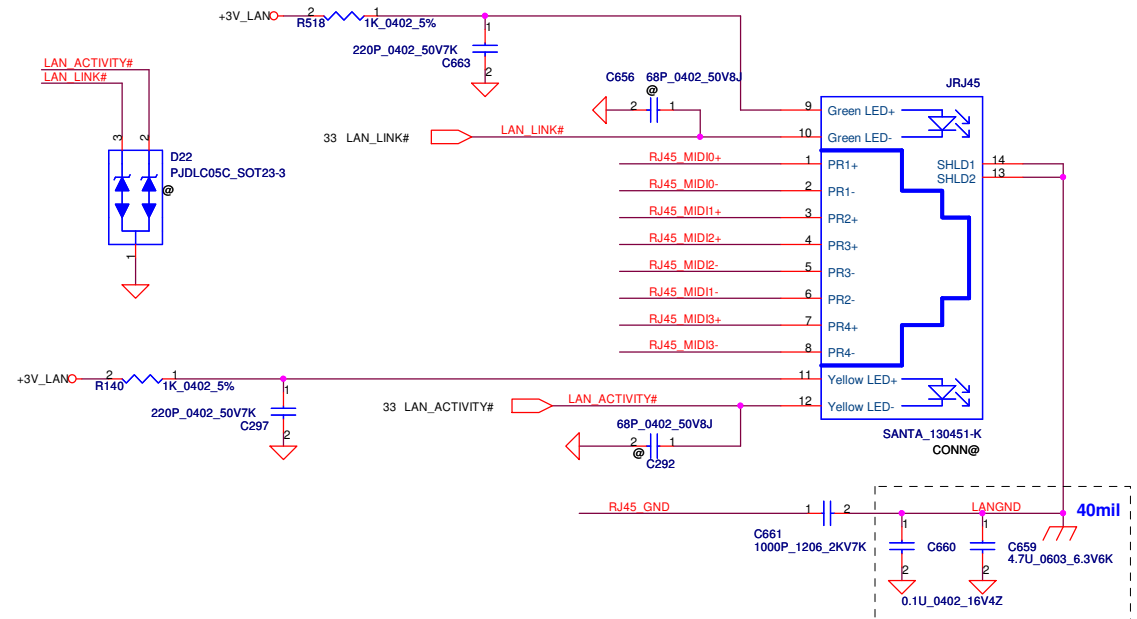
SM010005500 500ma 600ohm@100mhz DCR 0.38

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					Customer Part Number		
					Date:	Tuesday, December 29, 2009	Sheet 33 of 59
					NEW70 M/B LA-5891P Schematic		

## LAN Connector

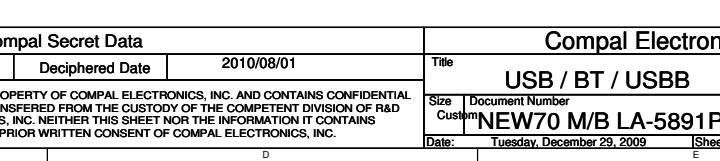
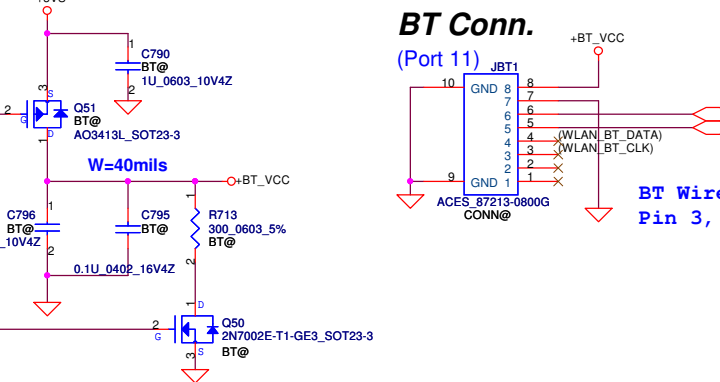
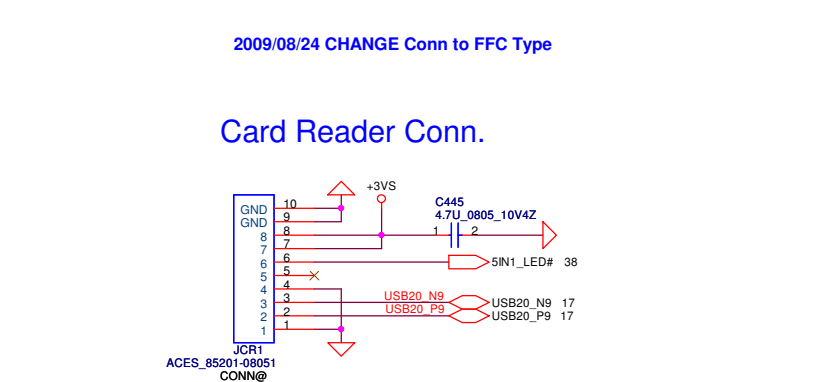
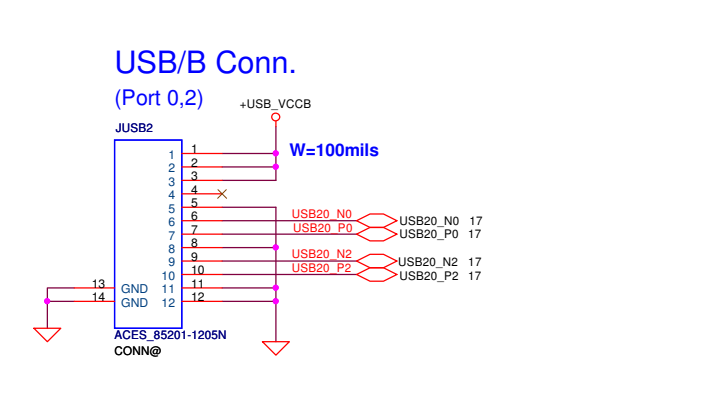
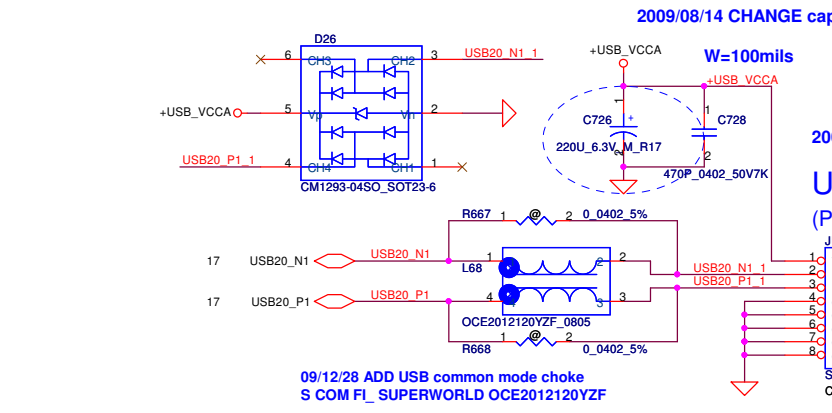
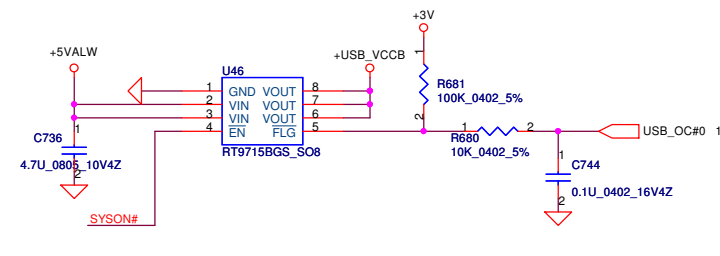
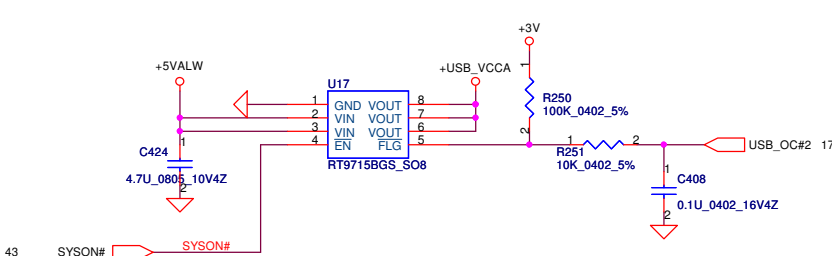


BOTHHAND: S X'FORM\_ GST5009-D LF LAN, SP050006B00  
TIMAG:S X'FORM\_ IH-160 LAN , SP050006F00



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				Date:	Tuesday, December 29, 2009	Sheet 34 of 59	



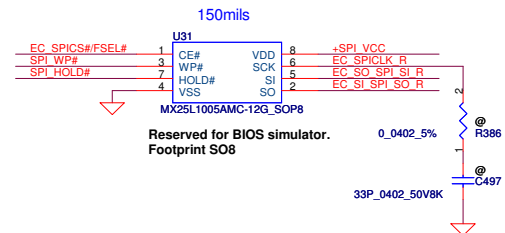
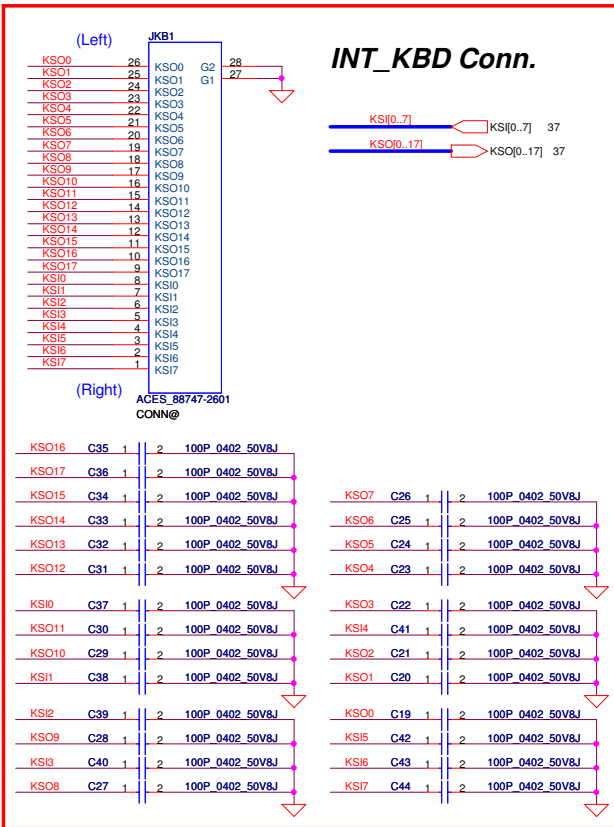
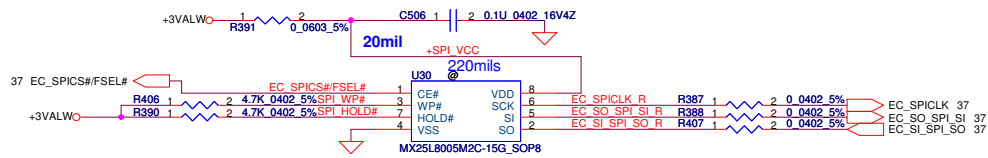


WWW.AliSaler.Com

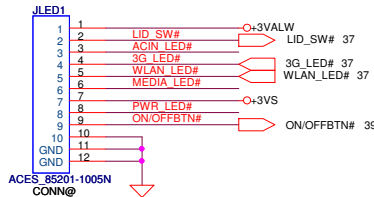
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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	
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Size	Document Number	Customer	NEW70 M/B LA-5891P Schematic	Rev	1.0
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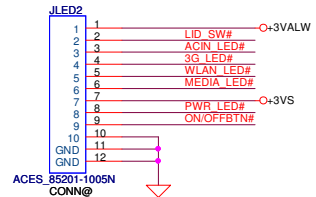




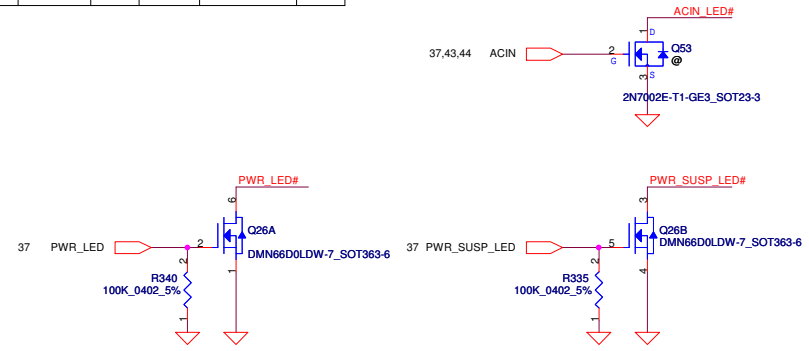
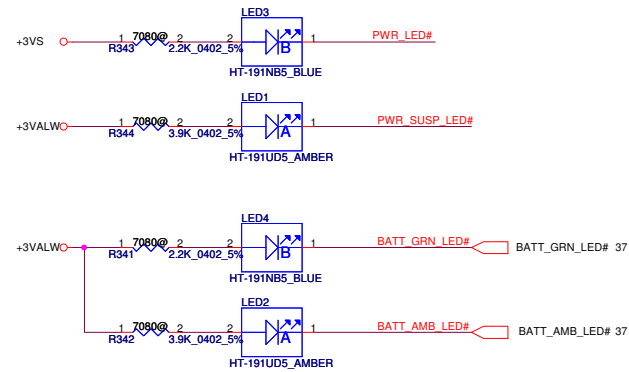
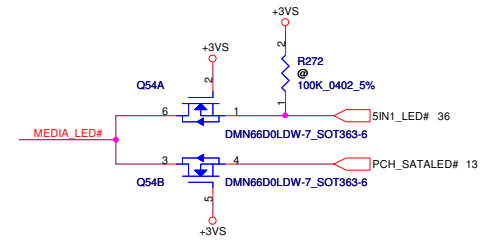
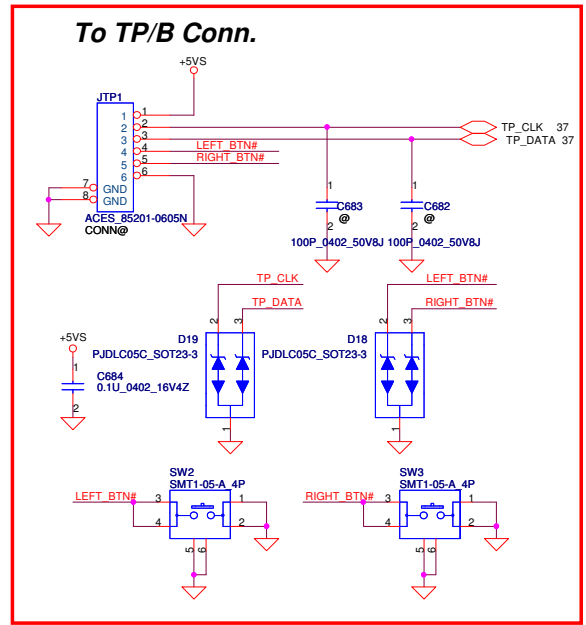
### LED/B RIGHT



### LED/B LEFT



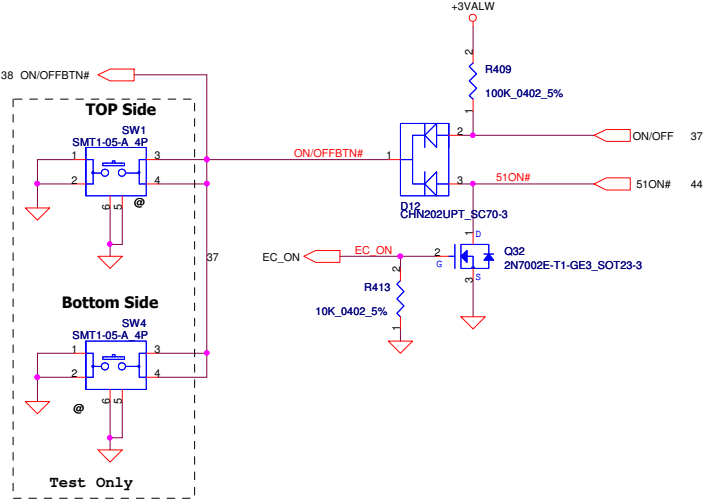
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		



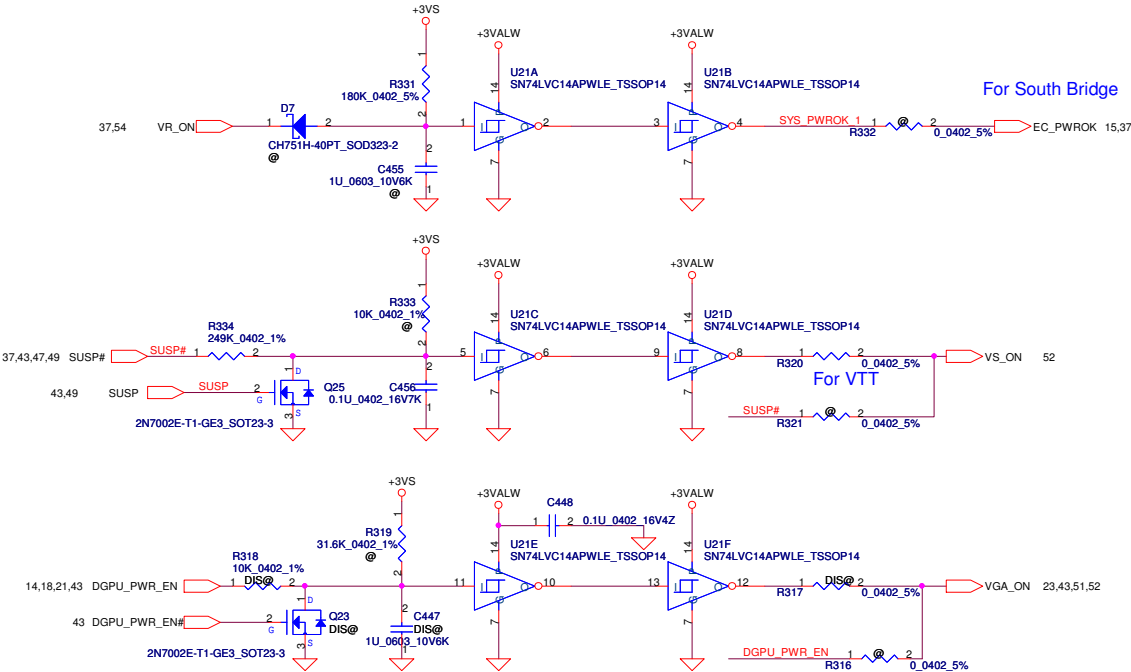
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	BIOS, I/O Port & K/B Connector
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Power Button

ON/OFF switch

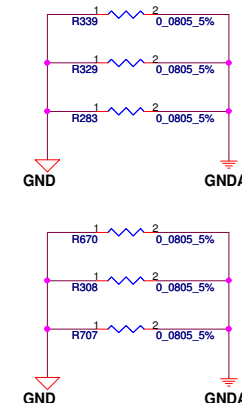
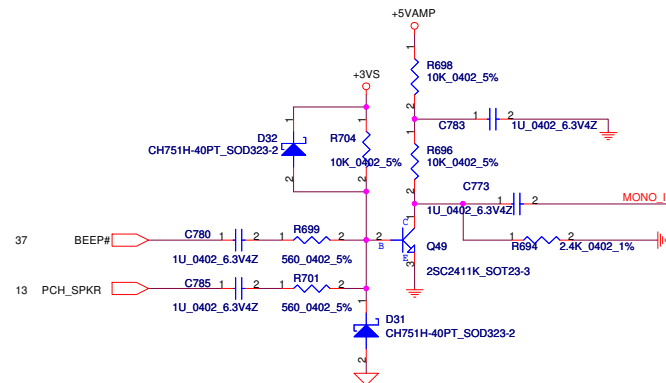
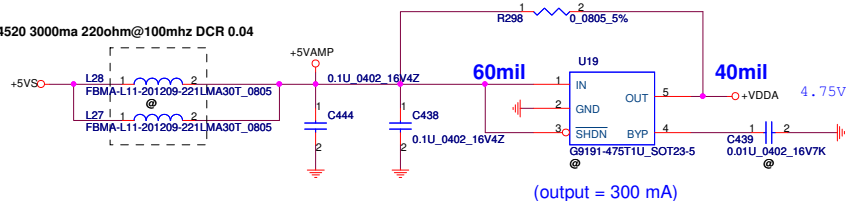


Power ON Circuit



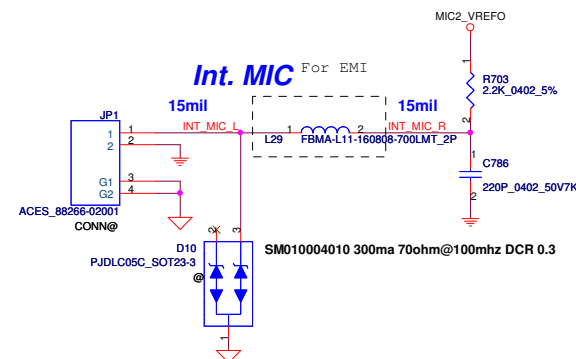
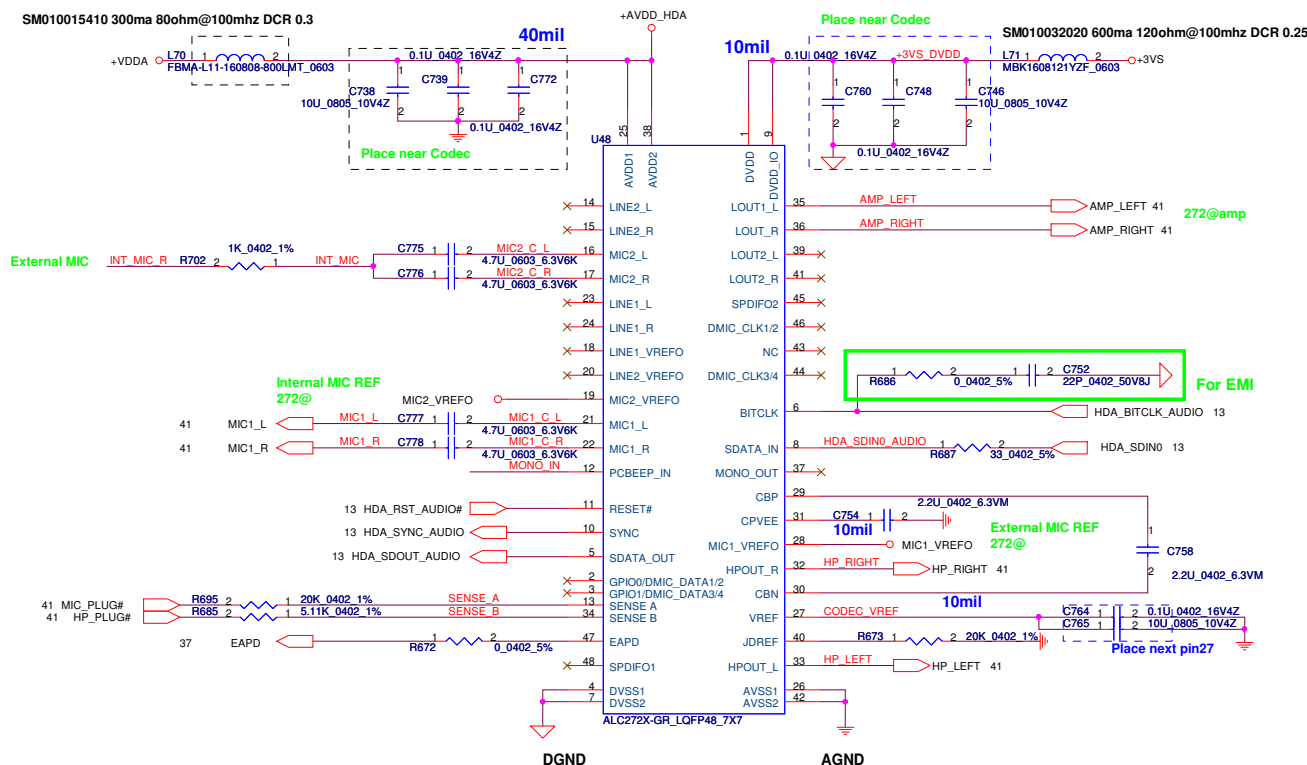
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						Document Number			
						NEW70 M/B LA-5891P Schematic			
						Rev			
						1.0			
						Date			
						Tuesday, December 29, 2009			
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SM010014520 3000ma 220ohm@100mhz DCR 0.04



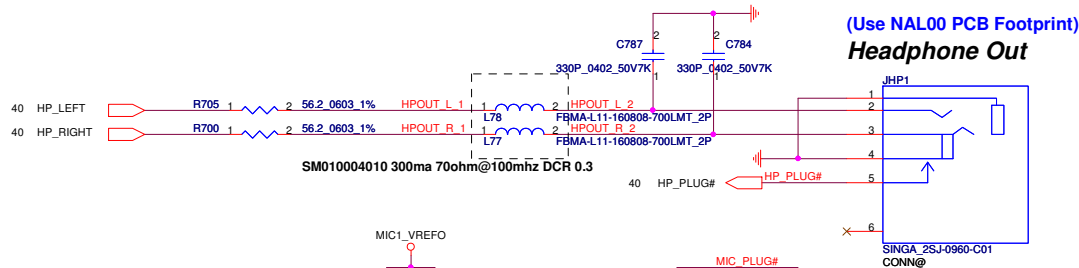
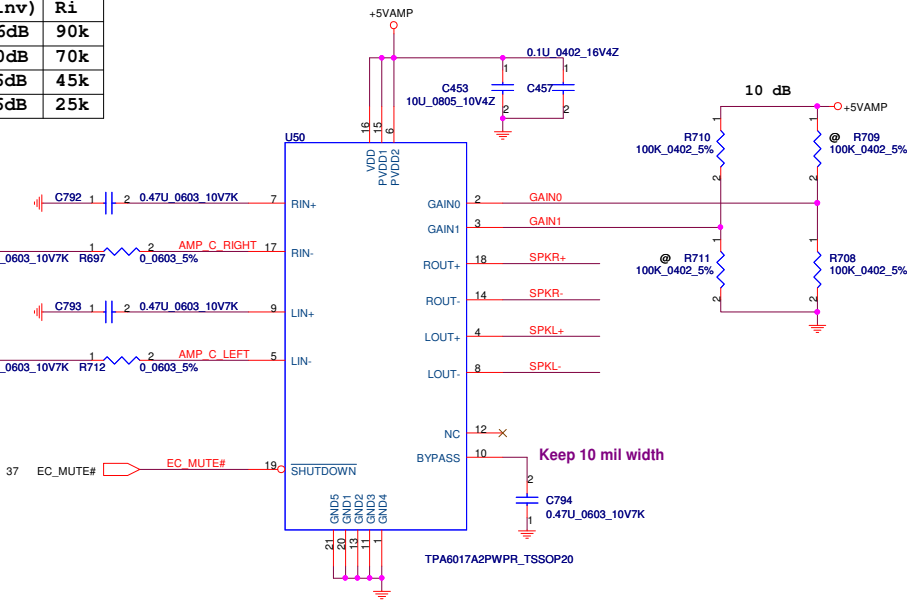
## HD Audio Codec

SM010015410 300ma 80ohm@100mhz DCR 0.3

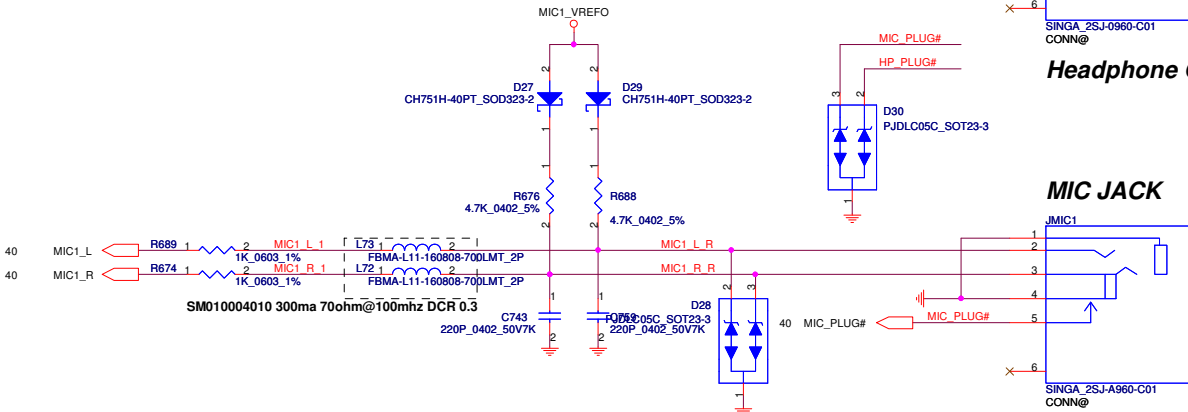
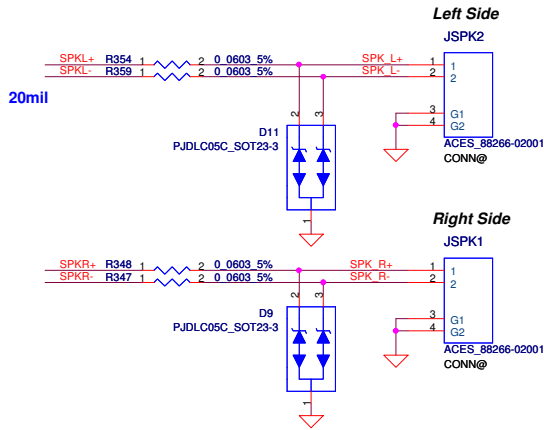


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GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

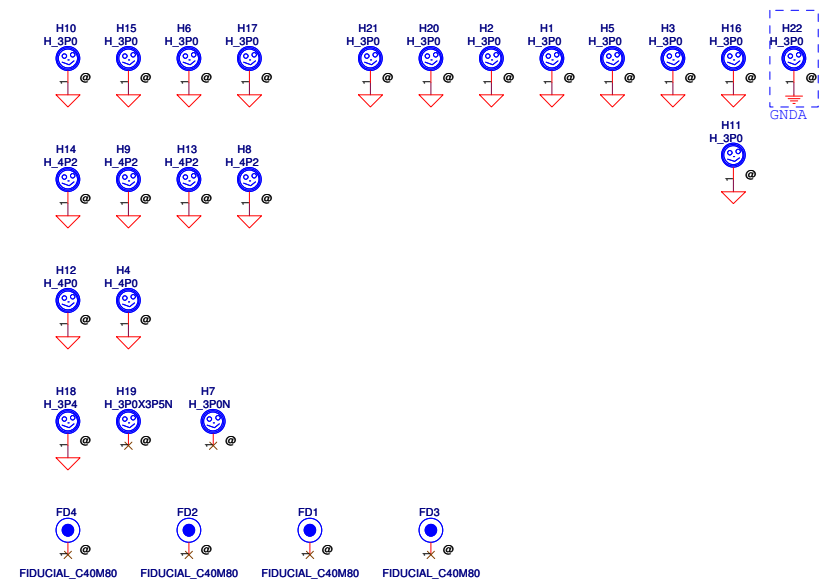
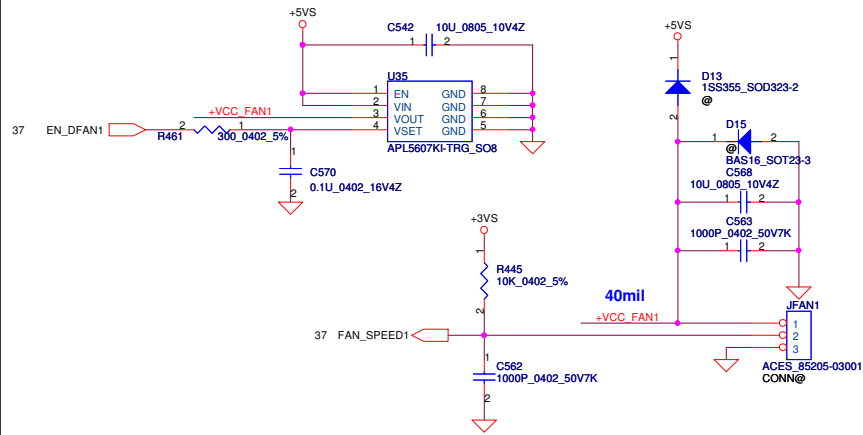


### Int. Speaker Conn.



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Deciphered Date				2010/08/01				Amplifier & Audio Jack			
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Document Number				NEW70 M/B LA-5891P Schematic				Rev 1.0			
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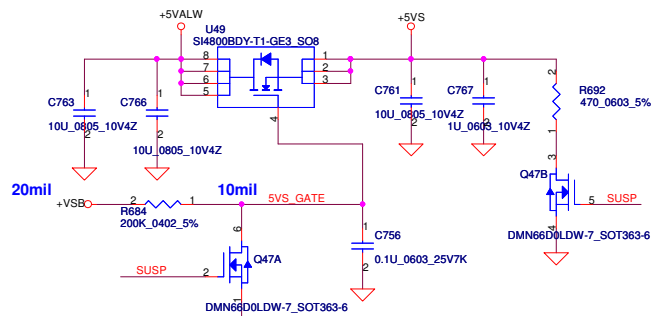
## FAN1 Conn



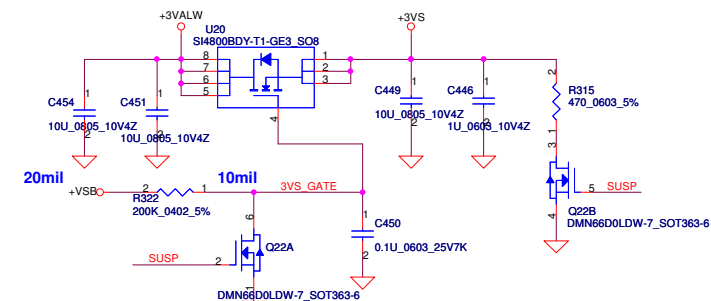
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	FAN & Screw Hole
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				Date:	Tuesday, December 29, 2009
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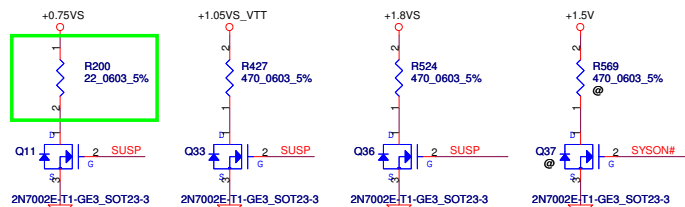
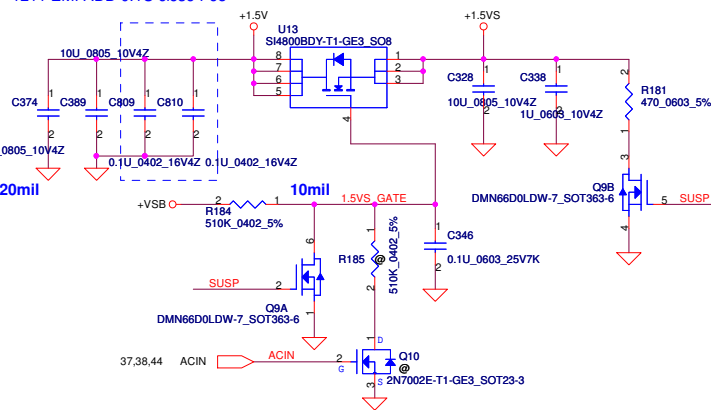
### +5VALW TO +5VS



### +3VALW TO +3VS

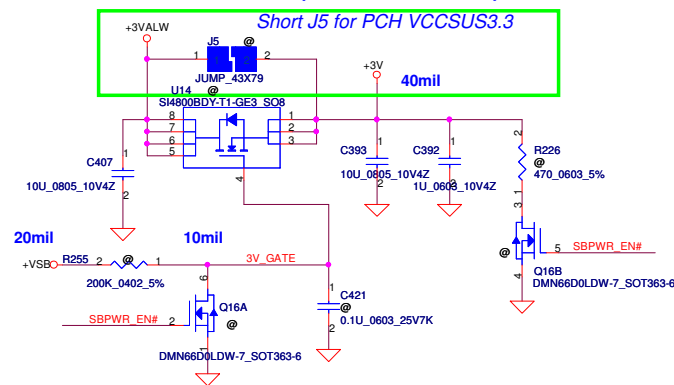


### +1.5V to +1.5VS

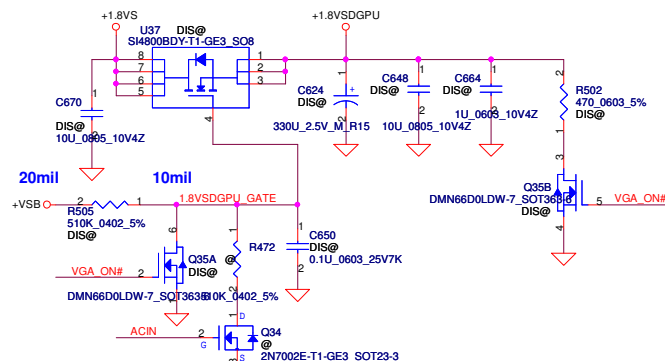


2009/08/14  
CP\_S3PowerReduction  
WhitePaper\_Rev0.9  
0.75VS speed up discharge

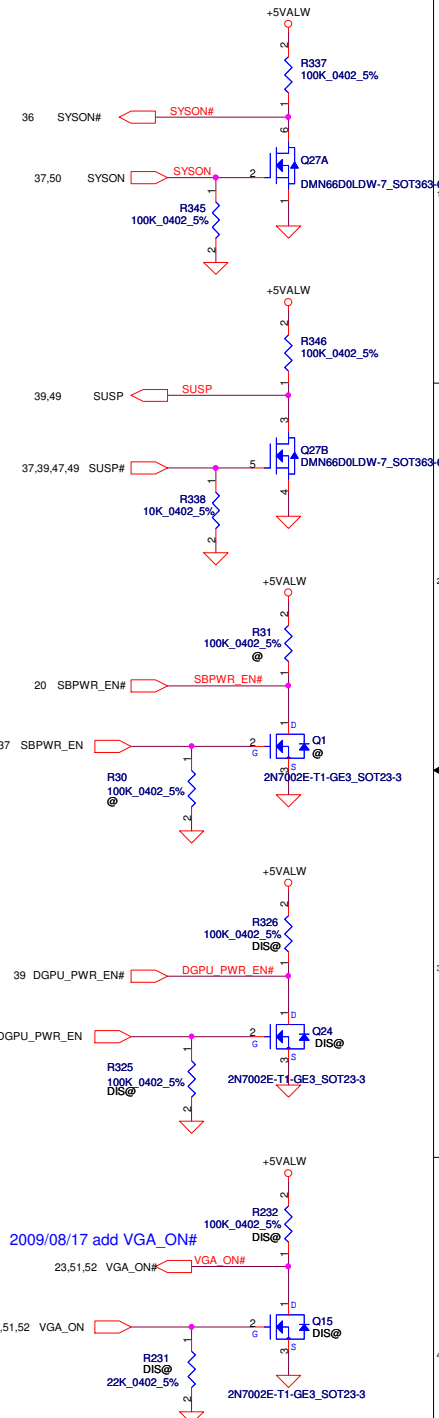
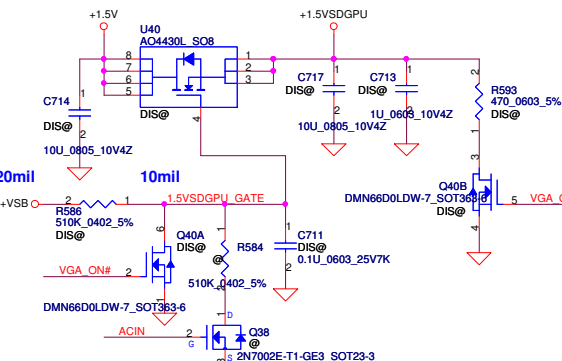
### +3VALW TO +3V(PCH AUX Power)



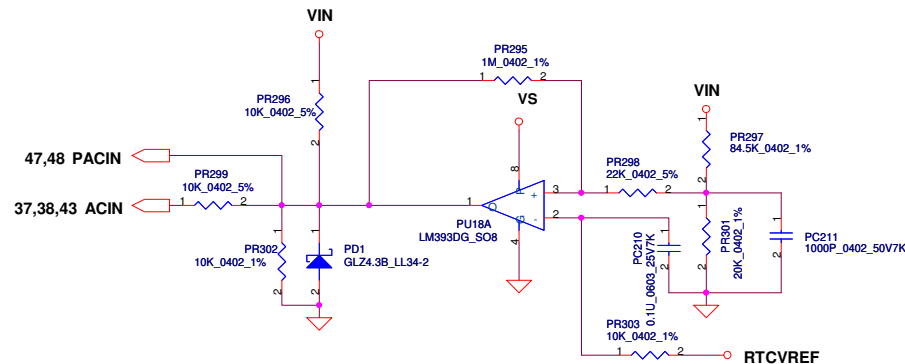
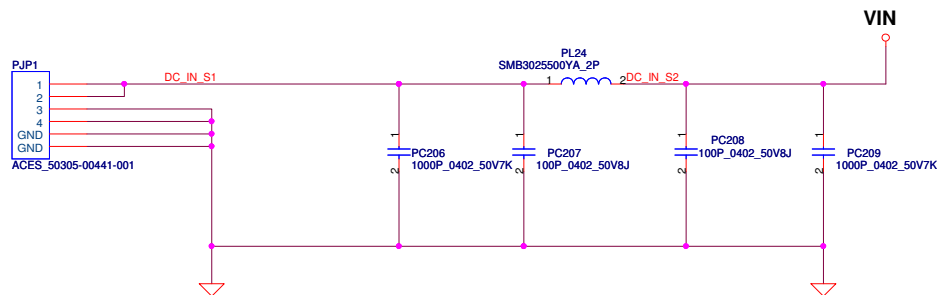
### +1.8VS to +1.8VSDGPU for GPU



### +1.5V to +1.5VSDGPU for GPU

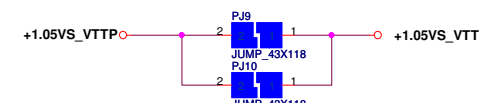
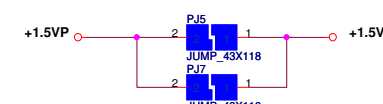
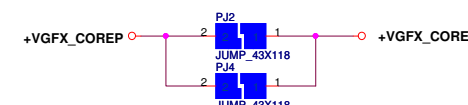
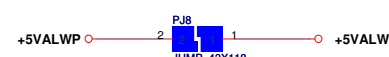
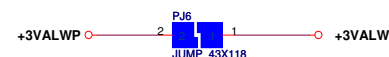
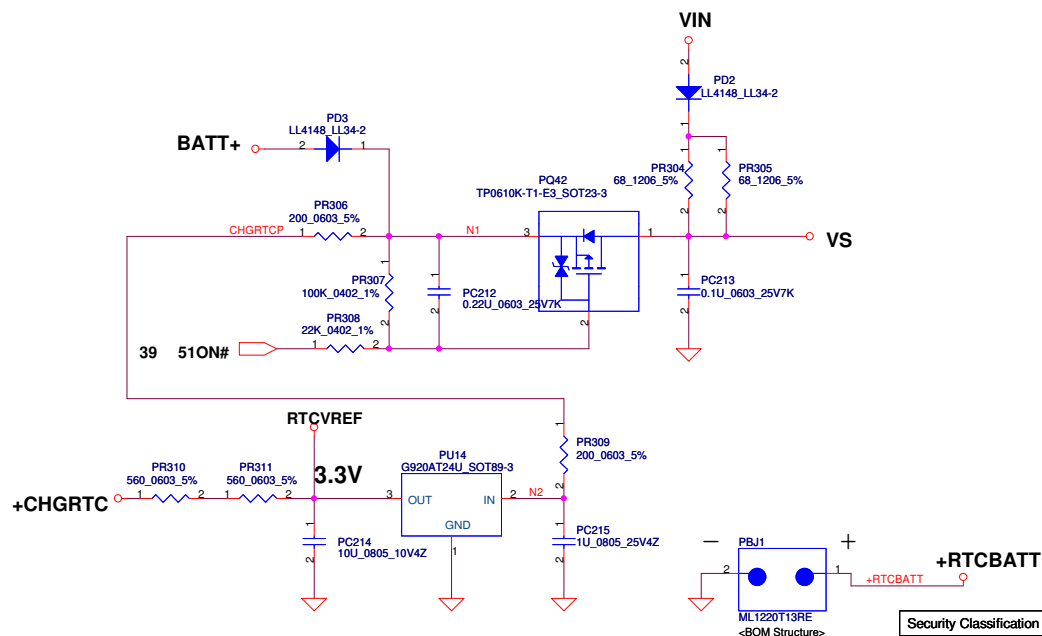


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						Document Number		Rev	
						NEW70 M/B LA-5891P Schematic		1.0	
						Date: Thursday, January 07, 2010		Sheet 43 of 59	

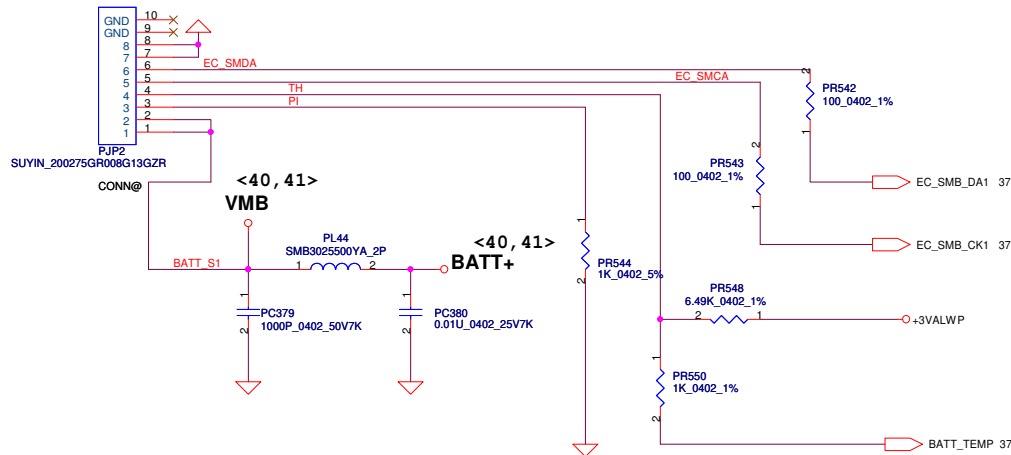


#### Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

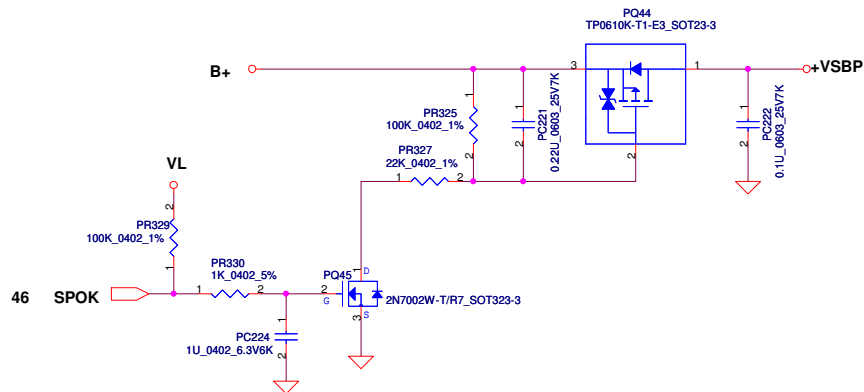
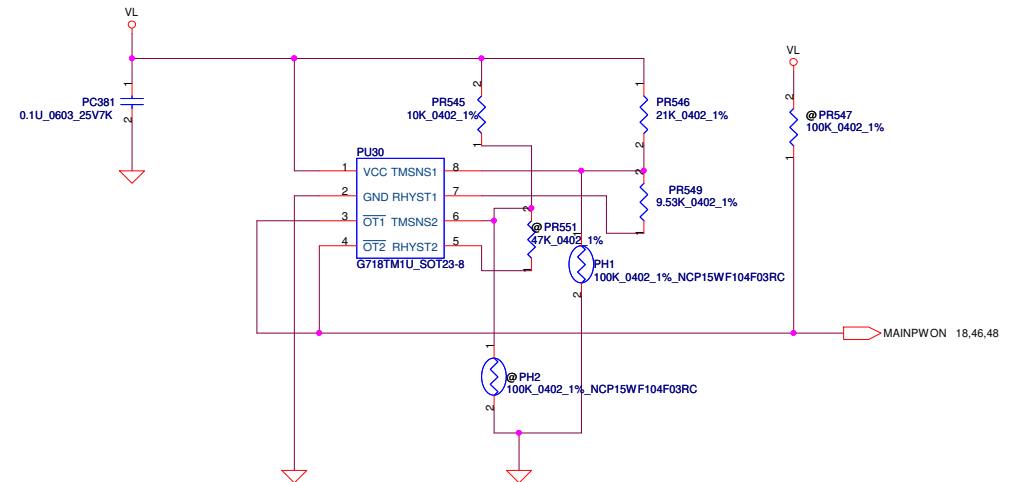


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2007/09/20				2010/08/01				Title			
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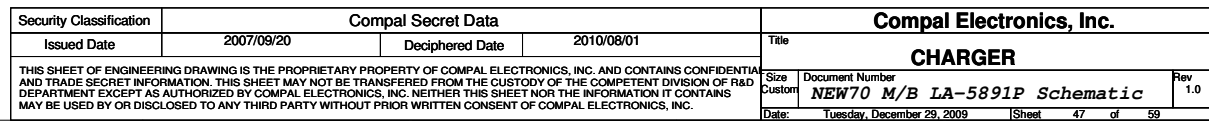
# PH1 under CPU botten side :

CPU thermal protection at 92 degree C  
Recovery at 56 degree C

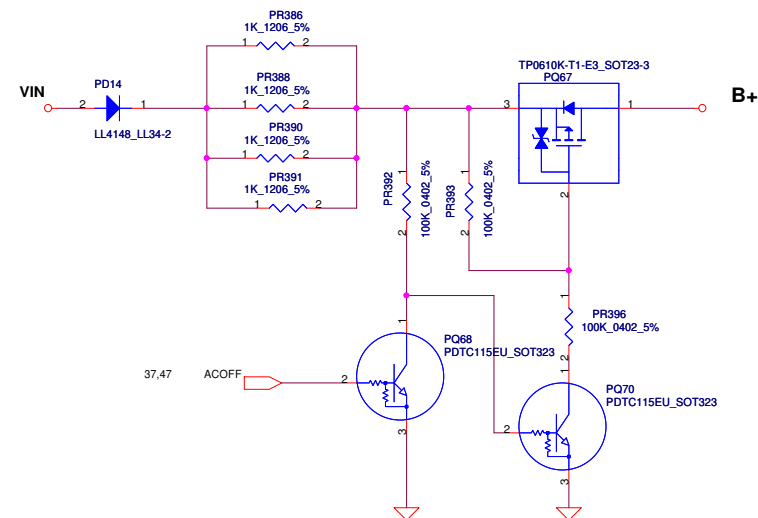


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$$\begin{aligned} \text{CP} &= 85\% \cdot I_{\text{ada}} ; \text{CP} = 4.07\text{A} \\ \text{CP} &= 85\% \cdot I_{\text{ada}} ; \text{CP} = 2.91\text{A} \end{aligned}$$






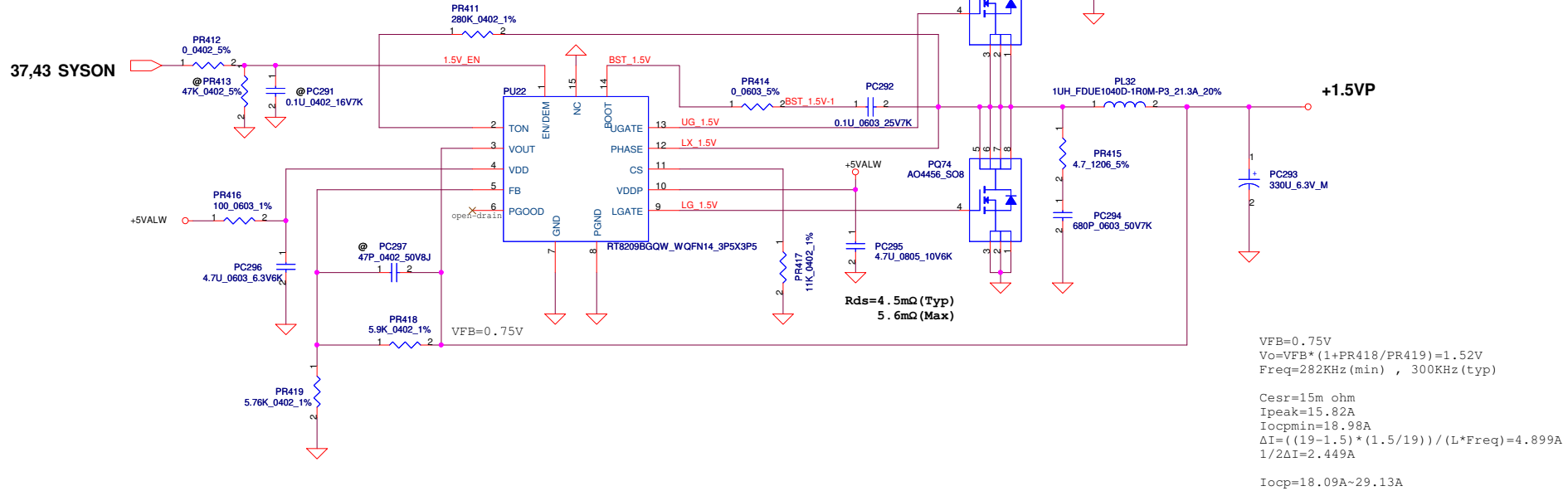
BATT ONLY			
	Precharge detector		
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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EN\_PSV  
 1. GND=>Disable SMPS  
 2. FLOAT=>PWM\_only mode  
 3. HIGH=>Auto\_skip mode

Because +1.5VSP has 17.74A power budget, it includes  
 DDR3, VGA chip, VRAM, so must use molding choke.



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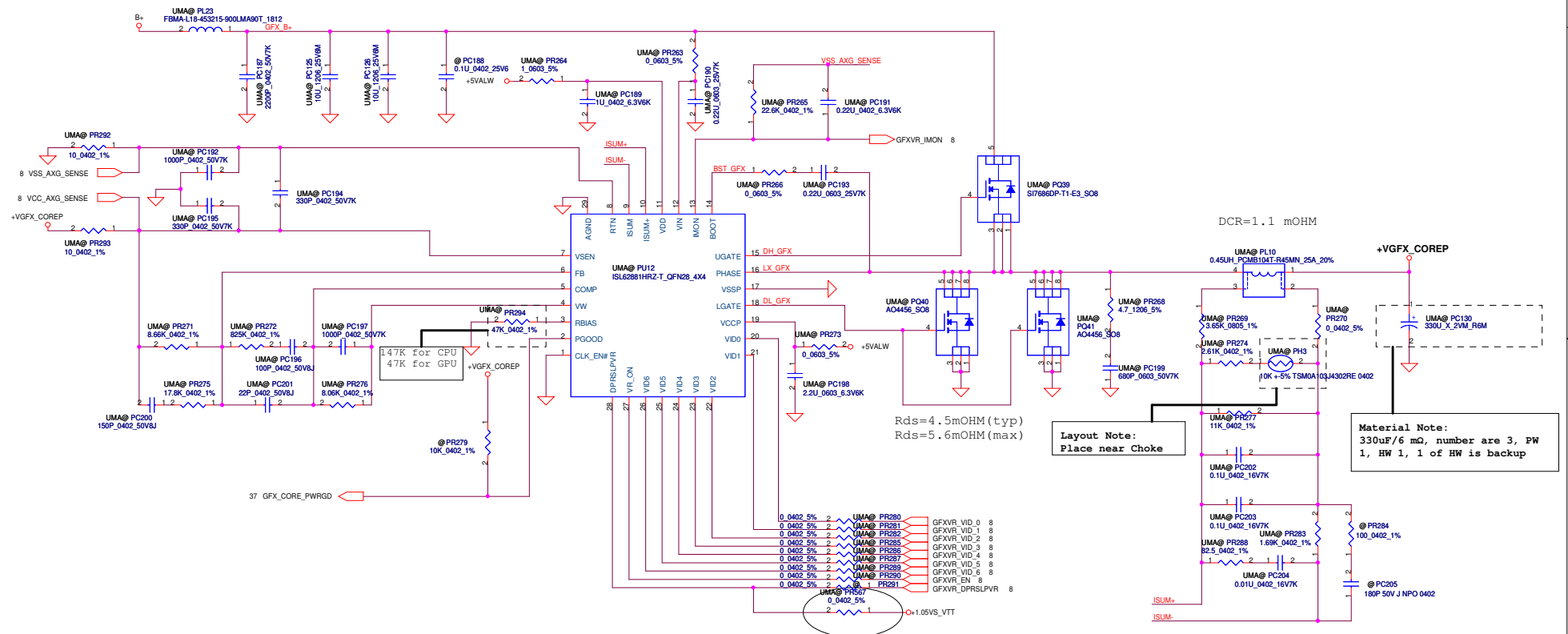




```

Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCF calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCF Threshold*Rdroop/LL=24.89A

```



2009-1214 common circiut modify.

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## Version change list (P.I.R. List)

Page 1 of 3  
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00( DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP ) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
14	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004080(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280.	2009-1029	to DVT
17	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC273 SE075103K80 PC275 SE000000I10 Delete PC272 SE107475K80, PC271 SE107105M80	2009-1029	to DVT
18	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Delete PR401 and PR403 SD028220280, PC274 SE026474K80 Change PR196 from SD034442280 to SD034365280.	2009-1029	to DVT
19	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PL14 from SL200000V00 to SH000005680 Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
20	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N SO8)	2009-1029	to DVT
21	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7686DP-T1-E3 1N POWERPAK SO8 )	2009-1029	to DVT
22	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323 )	2009-1029	to DVT
23	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU choke TOHO quality issue.	Because TOHO has quality issue before, change to Panasonic choke.	0.2	54	Change PL40/PL41 from SHSH00000F000 S COIL 0.36UH +-20% SF-I104-R36 23A to SH000005680 S COIL 0.36UH +-20% PCMC104T-R36MN1R17	2009-1029	to DVT
2	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	Change PR197 from SD034649280 to SD034432280.	2009-1029	to DVT
3	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	Chnage PR198 from SD034953180 to SD034887180.	2009-1029	to DVT
4	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	CHange PR201 from SD034316280 to SD034255280.	2009-1029	to DVT
5	+VGA_COREP, initial state unknow.	When VGA_CORE start up, but VBIOS doesn't ready, the VID is unknow, add pull down R.	0.2	51	Add PR557/PR560 SD028100280 ( S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
6	+1.0VSPDGPU, adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Change PC369 from SE076104K80 to SE000000K80 (S CER CAP 1U 0402 X7R)	2009-1029	to DVT
7	+1.0VSPDGPU, adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Change PR530 from SD028150380 to SD034270280 (S RES 1/16W 27K 0402 1%)	2009-1029	to DVT
8	+1.0VSPDGPU, adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Delete PR562 SD028220280 (S RES 1/16W 22K +-5% 0402)	2009-1029	to DVT
9	+0.75VSP, adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	49	Change PR409 SD028000080 to SD034249280 ( 24.9K 0402 1%)	2009-1029	to DVT
10	=1.8VSP, voltage too small.	Because +1.8VSP drop in HW side, increase +1.8VSP.	0.2	49	Change PC287 from SE076104K80 to SE000000K80	2009-1029	to DVT
11	+GFX_COREP, spike voltage issue.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	49	Change PR405 from SD034316380 (S RES 1/16W 316K +-1% 0402) to SD034309380 (S RES 1/16W 309K 0402 1%)	2009-1029	to DVT
12	+GFX_COREP, EMI request.	EMI request to add snubber.	0.3	53	Delete PD17 SCS00000Z00 ( S SCH DIO RB751V-40 SOD-323)	2009-1104	to DVT
13	+1.05VSV_VTTP, EMI request.	EMI request to add snubber.	0.3	53	Add PR268 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	2009-1104	to DVT
14	+VGA_COREP, EMI request.	EMI request to add snubber.	0.3	52	Add PC199 SE025681K80 (S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
15	+1.5VP, EMI request.	EMI request to add snubber.	0.3	51	Add PR465 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	2009-1104	to DVT
16	Charger, EMI request.	EMI request to add snubber.	0.3	51	Add PC332 SE025681K80 (S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
17	CPU_COREP, transient, load line modify.	CPU_COREP, transient, load line modify.	0.3	50	Add PR191 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	2009-1104	to DVT
18	+VGA_COREP, output voltage change.	Because ATI change Park output voltage, we saperate Park and Madison by PAK@ and MAD@. And Change Madison X63 BOM.	0.4	54	Add PC171 SE025681K80 (S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
19	+VSBP, EMI request.	EMI request to add cap to reduce EMI noise on B+	0.3	45	Add PR415 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	2009-1104	to DVT
20	+1.8VSP BOM error.	Loss +1.8VSP enable circiut.	0.3	49	Add PC294 SE025681K80 (S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
21	+CPU_COREP, power measure.	Because HW want to measure CPU_CORE IC power loss, Add 0805 R to saperate +5VS.	0.4	54	Add PR370 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	2009-1113	to DVT
22					Add PC262 SE074681K80 (S CER CAP 680P 50V K X7R 0402)	2009-1113	to DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	+CPU_COREP, IMON design change.	Intel release IMON RC time constant new request, change PC348 to 0.068u to meet spec.	0.4	54	Change PC348 from SE076103K80 S CER CAP .01U 16V K X7R 0402 to SE0000003J80 S CER CAP 0.068U 16V K X7R 0402	2009-1113	to DVT
2	+CPU_COREP, cost issue.	SF000000G80 will cost up, change to SF22004M210.	0.4	54	Change PC343 from SF000000G80 to SF22004M210.	2009-1113	to DVT
3	+3V/+5V cost issue.	Because Nippon cost up thier OS-CON cap, so we change Nippon cap to Sanyo cap by sourcer request.	0.5	46	Change PC233/PC237 from SF22001M300 S ELE CAP 220U 6.3V M F60(6.3X5.7) PXC to SF22001M200 S ELE CAP 220U 6.3V M B C6 SVPC ESR15	2009-1118	to DVT
4	+1.05VS_VTTP issue.	+1.05VS_VTTP choke unique to +1.5VP.	0.5	52	Change PL38 from SH000008V80 S COIL 1UH +-20% PCMB103E-1R0M20A to SH000009U00 S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A	2009-1118	to DVT
5	+VGA_COREP 2nd source issue.	In order to phase in 2nd source of APW7138, must add Pin6 components to meet ISL6268 requirement.	0.6	51	Add PC172 SE071220J80 S CER CAP 22P 50V J NPO 0402 Add PC174 SE075682K80 S CER CAP 6800P 25V K X7R 0402 Add PR195 SD034909280 S RES 1/16W 90.9K 0402 1%	2009-1208	to PVT
6	+VGA_COREP 2nd source issue.	In order to phase in 2nd source of APW7138, must add Pin6 components to meet ISL6268 requirement.	0.6	51	Change location PU23 to PU998.	2009-1208	to PVT
7	+1.05VS_VTTP 2nd source issue.	In order to phase in 2nd source, change ISL6268 to APW7138.	0.6	52	Change PU26 from SA00001HT80 S IC ISL6268CAZ-T SSOP 16P to PU999 SA000020600 S IC APW7138NITRL SSOP 16P	2009-1208	to PVT
8	+1.05VS_VTTP 2nd source issue.	APW7138 needn't pop PC335.	0.6	52	Delete PC335 SE075103K80 S CER CAP .01U 25V K X7R 0402 and change location to PC999.	2009-1208	to PVT
9	HDD LED flash issue.	HDD LED will flash when plug in adapter, because +3VS rise a little. HW request add PC224 to solve it.	0.6	45	Add PC224 SE000000K80 S CER CAP 1U 6.3V K X5R 0402	2009-1208	to PVT
10	HDD LED flash issue.	If add PC224, must change PR330 from 0 to 1K to avoid SPOK pin fail. that is add a current limit R on SPOK pin.	0.6	45	Chnage PR330 from SD028000080 to SD028100180.	2009-1208	to PVT
11	BOM error.	+1.8VSP choke use wrong material.	0.6	49	Change PL30 from SH000006I80 S COIL 2.2UH +-20% PCMC063T-2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A	2009-1208	to PVT
12							
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21							

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B --> B Change List

1012:-----  
Page 29,30 Update F1,F2 symbol to SP04301P120(F\_SMD1812P110TF)  
Page 36,38 C789,C788,C684 symbol update (have pin define)  
Page 31, U3 P/N change from SA00001RM00 to SA00003O900  
1102:-----  
Page 7,8 C97,C675,C134,C136,C251,C268,C541,C667 symbol update from SGA00002380 to SGA00002U00  
Page 23. Add C609 0.1u \_0402(SE076104K80) R739 24K \_0402(SD034240280) fix +3VSDGPU Ramp up issue  
Page 17,35 Add 1 more USB trace to 3G/B connector from PCH USB20\_P10 & USB20\_N10  
1103:-----  
Page 43 R200 change symbol from 22 \_0402 \_5% to 22 \_0603 \_5%  
Page 39 SW1,SW4 BOM structure change to @  
Page 36 C789.2 power source +3VS change to +3VALW  
1104:-----  
Page 8, Add C797,C798,C799,C800 0.1u \_0402 at between +1.5V&+1.5V\_1(Intel suggest)  
Page 15,37 U41.F3 modify net from GPIO62 to susclk  
Page 37 Add R740(@) close U32.123  
1105:-----  
Page 8 R98 change from 4.7K \_0402 \_5% to 330ohm \_0402 \_5% (Intel feekback VGFX\_CORE issue solution)  
1109:-----  
Page 23 Change R717,R718,R720,R509 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)  
Page 24 Change R64 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)  
Page 23 Remove and short R729 (A2VDD)  
Page 23 Change C600,C172,C599 BOM structure from VGA@ to @ (+A2VDD)  
Page 23 Remove and short L6 (+A2VDDQ)  
Page 26 Remove and short R730,R731,R732,R733,R734,R735,R736,R737,R738, (DPB,DPC,DPD power source)  
Page 37 Add R508 100K \_0402 Pull down to GND(EC E51TXD\_P80DATA)(fix Intel WLAN Card reset issue)  
RF request:-----  
Page 35 Add C801 (SE071470J80 47P \_0402) and C173(SE000005T80 10U \_0603)(+3VS\_WWAN)  
Page 23 Remove R508 (100 \_0402) change to C802(@) (12P \_0402 \_50V8J)(SE071120J80) (VGA\_CLK\_27M)  
Page 29 Add two shunt C804,C803 12P \_0402 \_50V8J(SE071120J80)(P31.DDC to HDMI conn)  
Page 29 Add two shunt C805,C806 22P \_0402 \_50V8J(SE071220J80)(P29.LCD Conn)  
pop R403(47 \_0402) and C516 (22P \_0402)(CLK\_PCI\_LPC)  
pop R163 (10 \_0402)and C319 (10P \_0402) (CLK\_BUF\_ICH\_14M)  
EMI request:-----  
Page 36 POP D26, CM1293-04SO(SC300000O00)  
Page 38,40,41 POP D18,D19,D10,D9,D11,D28,D30 PJDLC05C(SCA00001100)  
1110:-----  
Page 38 Add Q53(ACIN\_LED#)  
1111:-----  
Page 40 C775,C776,C777,C778 change Symbol from SE093475K80(4.7U \_0805) to SE107475M80(4.7U \_0603)  
Page 38 R341,R343 100 \_0402 \_5% change to 680 \_0402 \_5%(BLUE LED Bright)  
Page 38 R342,R344 300 \_0402 \_5% change to 3.9K \_0402 \_5%(Orange LED Bright)  
1113:-----  
Page 8 R98 change from 330 \_0402 \_5% to 470 \_0402 \_5%(SD028470080)  
Page 23 Change back R717,R718,R720,R509 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)  
Page 24 Change back R64 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)  
1116:-----  
Page 13 U41 change P/N from SA00003N700 to SA00003N7B0  
Page 34 T16 change P/N from SP050006C00 to SP050006B00  
1117:-----  
Page 58 Add HW PIR

B --> C Change List

1209:-----  
R679 change BOM structure to @  
D13,D15 change BOM structure to @  
Change R717,R718,R720,R509 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)  
Change R64 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)  
Add R729 0 \_0402(SD028000080,@)  
Add R730 0 \_0402(SD028000080,@) LOCAL\_DIM for Panel new feature  
Add R731 0 \_0402(SD028000080,@) COLOR\_ENG\_EN for Panel new feature  
Add R732 100K \_0402(SD028100380)LOCAL\_DIM PD to GND  
Add R733 100K \_0402(SD028100380)COLOR\_ENG\_EN PD to GND  
Q53 change BOM structure to @  
ADD Q54 2N7002DWH\_SOT363-6(SB00000AR10) for AC PLUG HDD LED flash issue  
DEL U16 for AC PLUG HDD LED flash issue  
C97,C134,C136,C251,C541,C268,C675,C667 symbol update from SGA00002U00 to SGA00001Q80  
C775,C776,C777,C778 change P/N SE107475M80 to SE107475K80(4.7U \_0603 \_6.3V6K)  
R272(100K PU +3VS) change BOM structure to @  
Add U32.85 WWAN\_LED# (input)  
Add U32.17 MINI1\_LED# (input)  
Add R734 PD to GND (fix PT Panel flash issue)

1211:-----  
ADD C807,C808 1000P \_0402(SE074102K80) LAN EMI  
ADD C610 0.1U \_0402 Y5V(SE070104Z80) VGFX\_CORE EMI  
ADD C809 C810 0.1U \_0402 Y5V(SE070104Z80) +1.5V EMI  
1211B:-----  
Add U32.36 WLAN\_LED# (output)  
Add U32.91 3G\_LED# (output)  
Add U32.85 WWAN\_LED# (input)  
1214:-----  
ADD R735 For U24 power source +3VS (POP)  
ADD R736 For U24 power source +5VS (@)  
1215:-----  
ADD R737 asmedia CLK-  
ADD R738 asmedia CLK+  
U24 PN change to SA00000U500 (74AHC1G125GW\_SOT353-5)  
1216:-----  
C465 change BOM structure to @(3G 150U)  
R41 change BOM structure to @(CRT DET)  
Q20 change BOM structure to @(CRT DET)  
R343,R341 change to 2.2K \_0402 \_5%(SD028220180) (LED)  
R334 change to 249K \_0402 \_1%(SD034249380)  
1217:-----  
R253 2.2K \_0402 \_5% change to @  
R252 2.2K \_0402 \_5% change to UMAHD@  
R343 change to 2.2K \_0402 \_5%(7080@) 680 \_0402 \_5%(90@)  
R344 change to 3.9K \_0402 \_5%(7080@) 680 \_0402 \_5%(90@)  
R341 change to 2.2K \_0402 \_5%(7080@) 680 \_0402 \_5%(90@)  
R342 change to 3.9K \_0402 \_5%(7080@) 680 \_0402 \_5%(90@)  
1219:  
R382 change to 18K \_0402(SD028180280)(Board ID)  
R389 ADD 100K \_0402 \_5%(SD028100380) PH +3VALW(Board ID)  
1223:  
R157 change to R167 10K \_0402 \_5% (GPIO66: L:6L H:8L)  
GPIO21 define to Project ID (L:NEW50/70/80/90 H:NEW71/91)

C --> MP Change List

1228:  
MB PCB P/N (DA80000H700)change to (DAZ0C900100)  
Q5,Q9,Q16,Q19,Q21,Q22,Q26,Q27,Q35,Q40,Q47,Q54 change SB00000AR10 to SB00000D900  
DEL D10 (Int. MIC ESD Diode PASS Can remove)  
R382 change to 18K \_0402 \_5%(SD028180280 Board ID rev0.3)  
DEL R667,R668(SD028000080) USb common mode choke  
DEL R167,(SD028100280)(GPIO66 PH 8L,PD 6L) 10K \_0402 \_5%  
ADD R157 (SD028100280)(GPIO66 PH 8L,PD 6L) 10K \_0402 \_5%  
ADD R389 (SD028100380)(Board ID)100K \_0402 \_5%  
ADD L68(SM070001600 12ohm bead) USB common mode choke  
Modify U24 Symbol  
  
0104:  
ADD R350 100K \_0402 \_5%(SD028100380)(3G PH +3VS\_WWAN)  
0107:  
Q5,Q9,Q16,Q19,Q21,Q22,Q26,Q27,Q35,Q40,Q47,Q54 change SB00000D900 to SB00000DH00

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								Size	Document Number						Rev
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## VGA

U34  
PARK@  
216-0774007 A11 PARK XT M2  
PARK XT M2 A11: SA00003MC10

## PCB

ZZZ  
LA-5891P MB Rev0: DA80000H700  
LA-5891P MB Rev1: DA80000H710  
LA-5891P MB with Small Board Rev1: DAZ0C900100  
LA-5891P REV1 M/B

## X76

ZZZ  
X761@  
X76198BOL01  
X76198BOL01 VRAM 512M SAM NEW70  
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

ZZZ  
X762@  
X76198BOL02  
X76198BOL02 VRAM 512M HYN NEW70  
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V )

ZZZ  
X763@  
X76198BOL03  
X76198BOL03 VRAM 1G SAM NEW70  
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

ZZZ  
X764@  
X76198BOL04  
X76198BOL04 VRAM 1G HYN NEW70  
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V )

ZZZ  
X765@  
X76198BOL05  
X76198BOL05 VRAM 512M AMD NEW70  
AMD :SA00003PF10  
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

ZZZ  
X766@  
X76198BOL06  
X76198BOL06 VRAM 1G AMD NEW70  
AMD :SA00003PF10  
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

## CRT Option Components

C607 C592 C567  
DIS@2 DIS@2 DIS@2  
15P\_0402\_50V8J 15P\_0402\_50V8J 15P\_0402\_50V8J

C603 C593 C569  
DIS@2 DIS@2 DIS@2  
12P\_0402\_50V8J 12P\_0402\_50V8J 12P\_0402\_50V8J

15P\_0402\_50V8J: SE071150J80  
12P\_0402\_50V8J: SE071120J80

L47 DIS@ 0\_0805\_5%  
L40 DIS@ 0\_0805\_5%  
L38 DIS@ 0\_0805\_5%

0\_0805\_5%: SD002000080

## NEW90 LED Option

2 5090@1  
R343 680\_0402\_5%  
2 5090@1  
R344 680\_0402\_5%  
2 5090@1  
R341 680\_0402\_5%  
2 5090@1  
R342 680\_0402\_5%

## PCH SKU Option

2 10K\_0402\_5%  
R259 UMAO@

GPIO19

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